mood-book

UNIT-II

BJT'S

* Bipolar Junction transistor:- Transistor is a silicon or germanium crystal with three distinct regions, Basically it consists of two P-N junctions connected back to back in a single piece of a semiconductor crystal. A Junction transistor is simply a sandwich of one type of semi-conductor material between two layers of the other type.

→ A transistor can be of two types (i) PNP (ii) NPN.

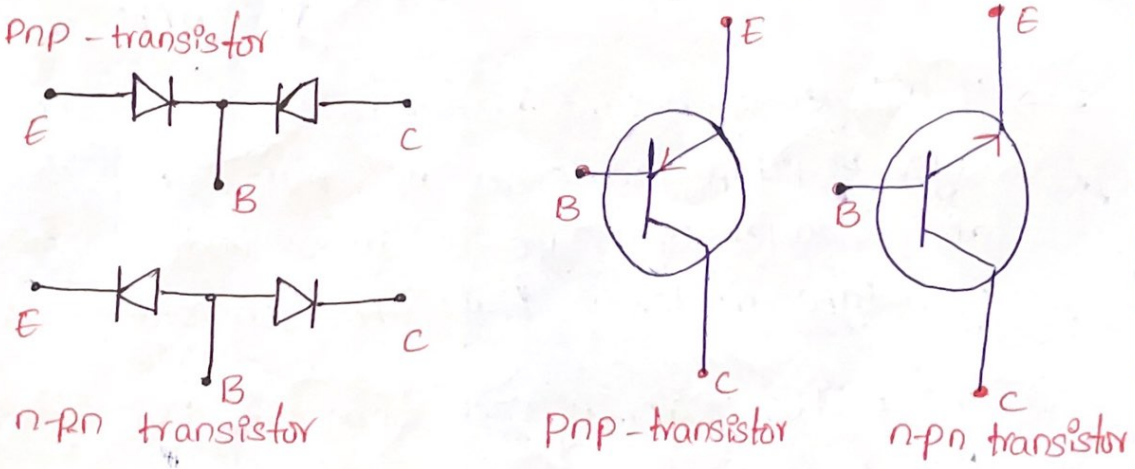
→ If a layer of n-type is sandwiched between two layers of P-type materials it is called pnp transistor, and a layer of P-type is sandwiched blw two layers of n-type material, it is npn transistor.

→ The middle region of each transistor type is called the BASE (B) & it is very thin (10^{-6}m) and very lightly dopped. The remaining two regions are called EMITTER (E) and COLLECTOR (C). The Emitter is heavily doped than other regions. It is physically larger than the base region and slightly smaller than collector region. Its main function is to supply majority charge carriers to the base. The collector is also heavily doped region than the base &

slightly lower than that of Emitter. It is physically larger than other regions. Its main function is to collect majority charge carriers through the base.

A transistor has two p-n junctions. one is b/w the Emitter and base called Emitter-base junction or simply Emitter junction (J_E). The other one is b/w base and collector called collector junction (J_C).

Thus a transistor is called, Junction transistor.



→ The main principle of a transistor is transfer of resistance, thus has given the name

Transfer resistor = Transistor

→ The current conduction in a transistor, generally. is because of both the types of charge carriers electrons and holes. Hence the name Bipolar Junction transistor (BJT).

→ If the current conduction is due to one type of carriers then it is called unipolar Junction transistor

* In the transistor symbol, the arrow head is always at the Emitter. It indicates the conventional current flow direction. i.e In case of PNP transistor it is from Emitter to base, while in case of npn transistor it is from base to emitter.

Because of difference in the size of the three regions and different dopping levels. There is no possibility of exchange of collector and Emitter terminals of a transistor in an Electronic circuit.

→ When transistor is formed difussion of charge carriers take place due to the charge gradient. During the diffusion the depletion region penetrates more deeply in to the lightly dopped region.

As shown in the figure depletion layer at the Emitter Junction penetrates more in to base region than the heavily dopped Emitter.

lly, at the collector junction depletion layer penetrates more into the base region than the heavily dopped collector. It should be remember that, as collector is slightly less dopped than the emitter, the depletion layer width at the emitter junction, inside the emitter is less than the depletion layer width at the collector junction inside the collector.

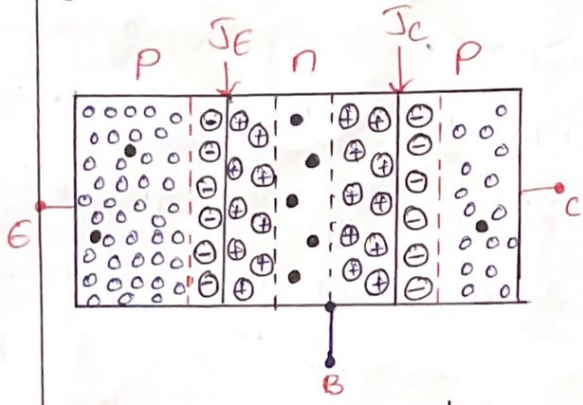


fig:- PNP transistor

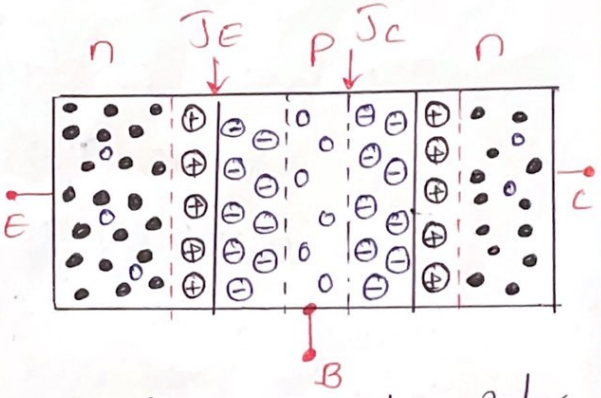
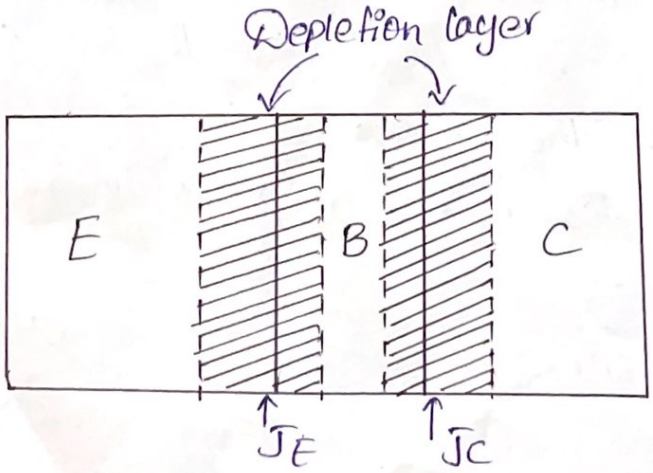


fig:- NPN transistor



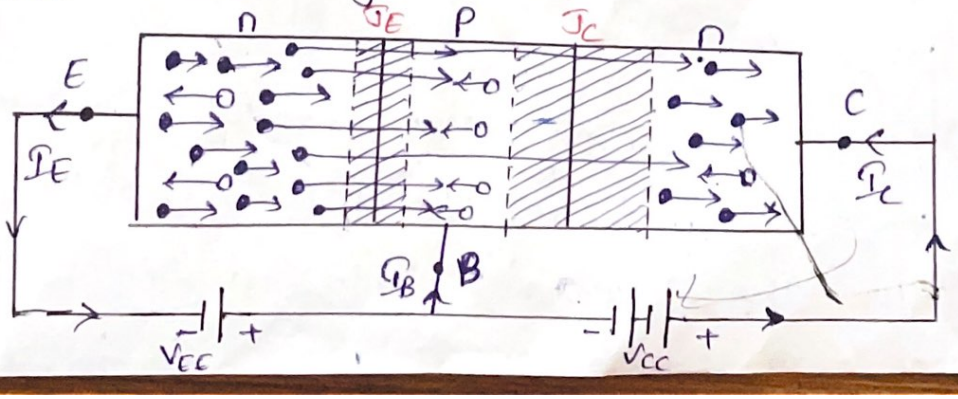
P-n Junction

* Operation of BJT :-

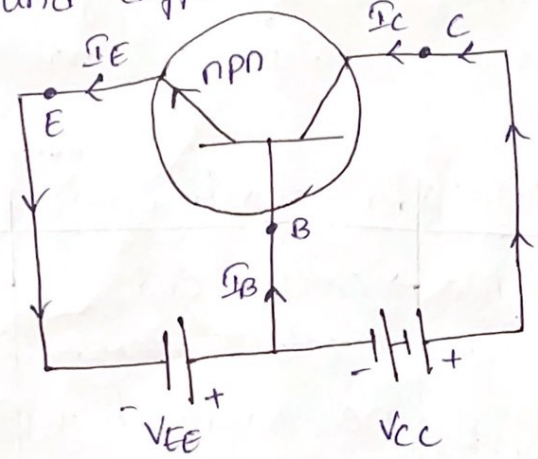
A :- **Biasing :-** for proper operation of a transistor, it is necessary to apply external voltages of correct polarity across its two junctions. Depending up on external voltage polarities used, the transistor works in any one of the three regions. they are Active, saturation and cut-off regions.

For Active region	for saturation region	for cut-off region
→ Emitter junction is forward bias → collector junction is reverse biased	→ Emitter and collector junctions are forward biased	→ Emitter and collector Junction are reverse biased.

B. **Working of npn transistor :-** the fig : shows the npn transistor with emitter Junction forward biased by a dc source V_{EE} and the collector Junction reverse biased by another dc source V_{cc}.



Due to the forward bias between emitter and base the width of the depletion layer at the Emitter Junction is reduced. i.e. the electrons of n-region (Emitter) are repelled by the negative potential of the External source and the potential barrier at this Junction is reduced and hence electrons cross the Junction and diffuse into P.region i.e - base.



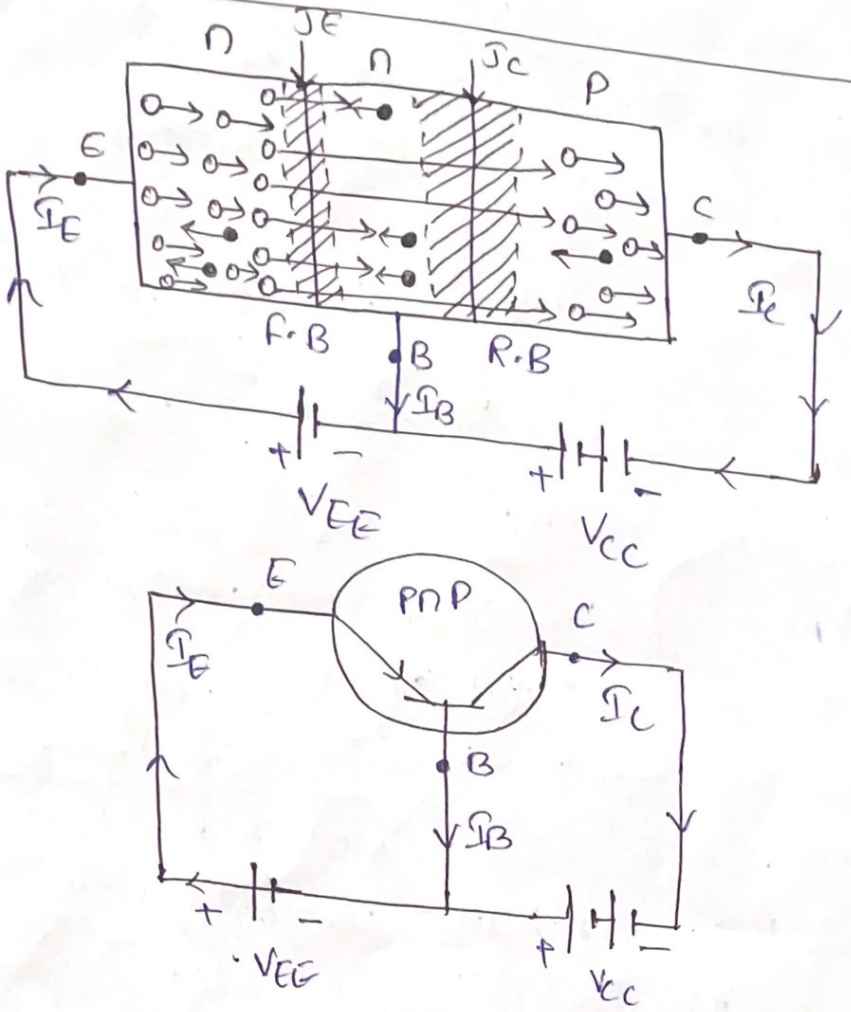
This constitutes the emitter I_E. the width of the base is very thin and is lightly doped. As these electrons flow through the p-type. base, they tends to combine with holes in base region. only 2% to 5% of emitted electrons will recombine with the holes in base region. This constitutes the base current I_B.

The remaining large no. of electrons (95% to 98%) are able to drift across the base and enter the collector region. And then electrons are

sweep by the positive potential of external source V_{cc}. This constitutes collector current I_c.

C. Working of pnp transistor :- consider a pnp transistor with Emitter Junction forward bias and collector Junction reverse biased.

The holes of Emitter (P-type) region are repelled by the positive potential of source V_{EE} towards the base. The potential barrier at Emitter Junction is reduced as it is forward biased and hence the holes cross this Junction and penetrate into n-type base region. This constitutes the Emitter current I_E. The width of the base is very thin & is lightly dopped, hence only 2% to 5% of the holes recombine with the free electrons in n-region. This constitute I_B (base current). The remaining large number of holes i.e 95% to 98%, are able to drift across base and enter collector. They are sweep by the negative collector voltage V_{cc}. This constitutes the collector current I_c.



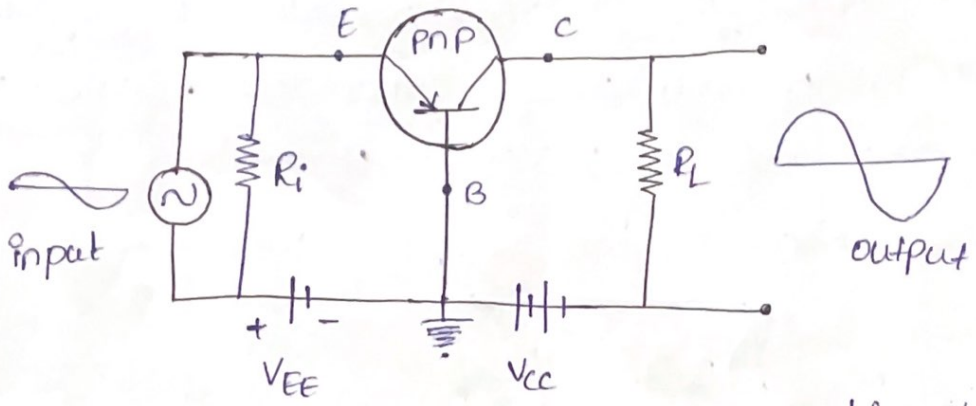
As each hole reaches the collector terminal, an electron is emitted from the negative terminal of the source V_{cc} and neutralizes the hole. At the same time a covalent bond near the emitter terminal breaks down and generates electron-hole pair, the new liberated electron leaves the emitter terminal and enter the positive terminal of the source V_{EE}. The new hole immediately moves towards the emitter junction and the process continues.

∴ Holes are the current carries in pnp transistor.

& current conduction is carried out by electrons.

* TRANSISTOR AS AN AMPLIFIER :-

Consider a PNP transistor as shown.



Here the Emitter Junction is forward biased and the collector Junction is reverse biased. The input signal is applied between the Emitter and base and the output is obtained across the load R_L connected between collector and base.

→ When an ac is fed to the input, during the positive half-cycle, increases the forward bias of the Emitter Junction which causes the more holes to flow. Consequently, Emitter current and collector current increases. These current variations produces corresponding voltage variations across the load R_L. Thus, the voltage drop across the load R_L also increases.

Ely during the negative half cycle of ac causes the transistor current to decrease. Since the Emitter Junction

Junction is forward biased, the depletion region around this Junction is much smaller than that around collector Junction which is reverse biased. consequently, the internal resistance R_{EB} of Emitter Junction is much smaller than the internal resistance R_{BC} of collector junction. Hence the power dissipation in the collector Junction is

$$P_{BC} = I_C^2 R_{BC}$$

The power dissipated in the Emitter Junction is

$$P_{EB} = I_E^2 R_{EB}$$

But. $I_C \simeq I_E$ & $R_{BC} >> R_{EB}$.

Hence $$P_{BC} >> P_{EB}$$

∴ The power dissipated at the Emitter Junction is much lower than the power dissipated at collector junction.

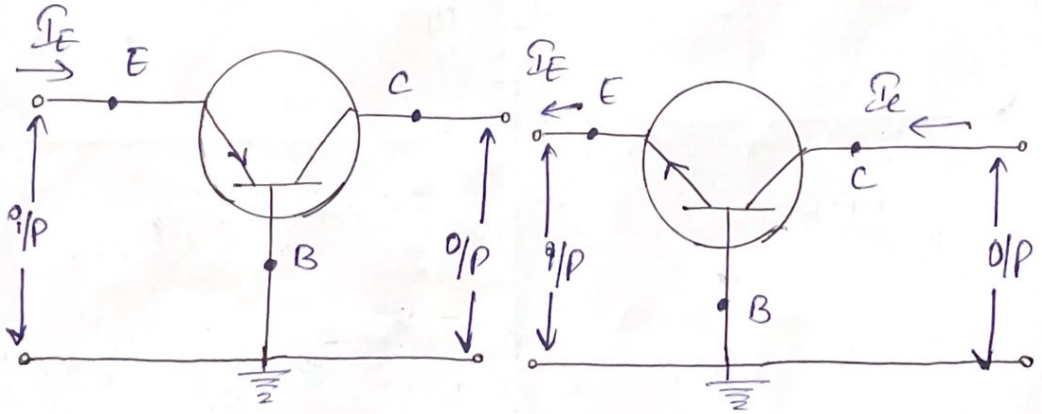
O/P power is >>> input

* Transistor configurations :-

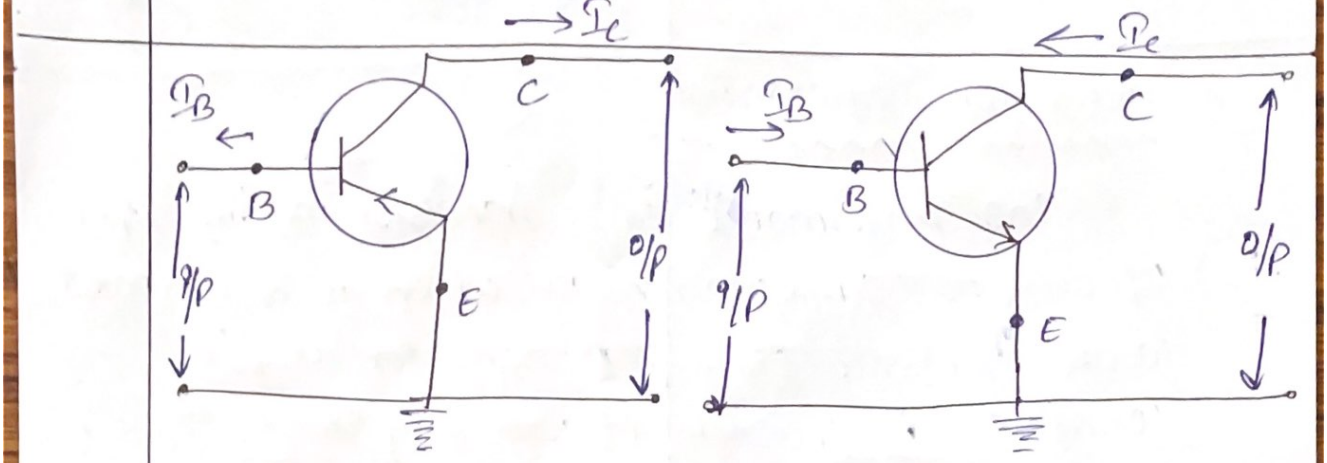
The performance of a transistor mainly depends up on the configuration in which it is connected in an electronic circuit. A transistor may be connected in the circuit with any one of its terminal common to both i/p & o/p. The common terminal is usually grounded. Accordingly a transistor may be operated in any one of the following configuration.

1. Common - Base configaration (CB)
2. Common - Emitter configuration (CE)
3. Common - collector configuration (CC)

PNP transistor npn transistor



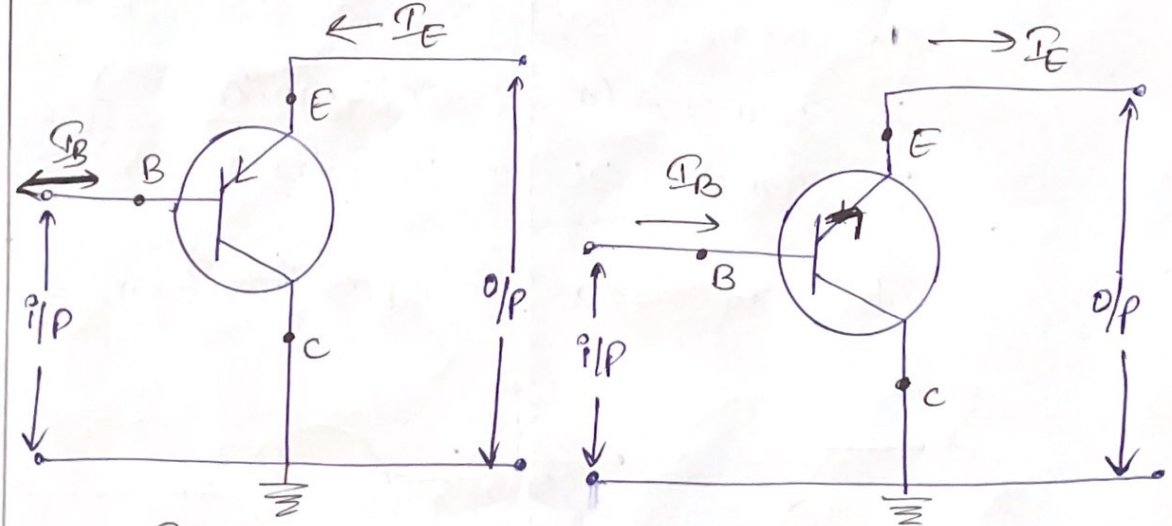
1. Common Base configuration.



PnP

nPn

2. Common Emitter configuration.



PnP

nPn

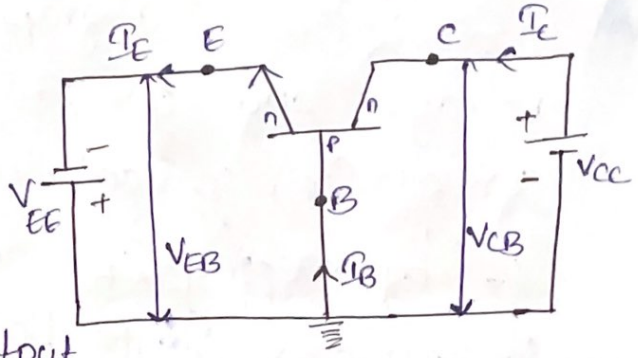
3. Common-collector configuration.

* Common Base configuration :- In this configuration Emitter is input terminal, collector is output terminal Base is common terminal.

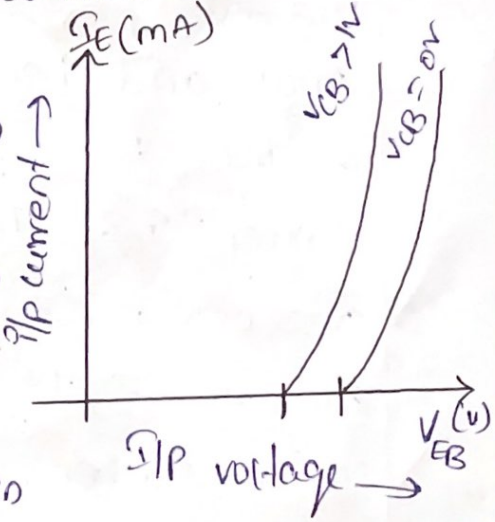
Input	output	common
Emitter	collector	Base

→ Input characteristics :-

Input characteristics are drawn between o/p voltage and i/p current by keeping output voltage constant. i.e Graph is drawn between V_{EB} & I_E by keeping V_{CB} constant.



When V_{CB} = 0V, the EB Junction is forward biased as shown in the characteristics, The Junction behave as a forward biased diode so that I_E increases rapidly with small increase in V_{EB}.

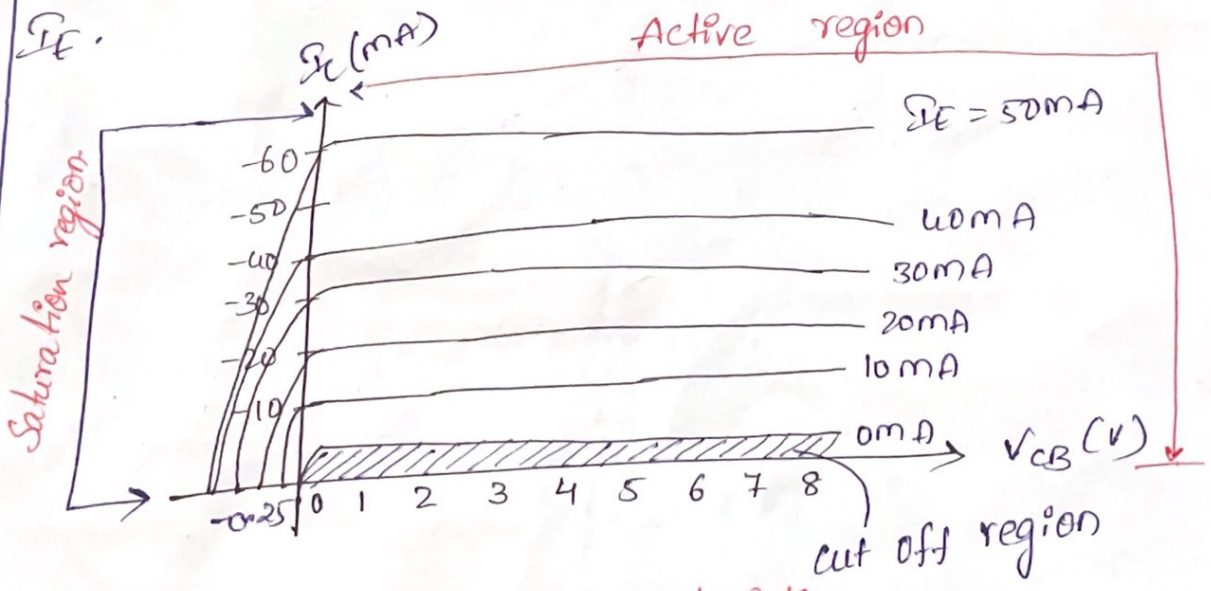


CB - i/p characteristics

When V_{CB} is increased, the width of base region is decreased. This effect result in increase of I_E. Therefore the curve shift towards left as V_{CB} is increased.

* Output characteristics :- To determine output characteristics, a graph is drawn between output voltage and output current by keeping input current (I_E) constant. i.e, graph between V_{CB} and I_C by keeping I_E constant.

This is repeated for different fixed value of I_E.



CB output characteristics

From the characteristics it is seen that for a constant value of I_E, I_c is independent of V_{CB} and curves are parallel to the axis of V_{CB}. further I_c flows even when V_{CB} equal to zero.

→ As the emitter-base junction is forward biased, the majority carriers, i.e, electrons, from the Emitter are injected in to the base region. Due to action of the internal potential barrier at the reverse biased collector-base junction. They flow to the collector region and gives rise to I_c even V_{CB} equal to zero.

Early Effect:- As the reverse bias across the collector to base junction increases, the depletion region width across the CB junction increases. with the result that the effective width of the box decreases. This dependency of base width on collector to emitter voltage is known as the Early Effect.

Due to Early Effect

→ There is less chance for recombination with in the base region, I_c increases with increasing V_{CB}.

→ for extremely large voltage, the effective base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called "punch through".

→ Output characteristics divided in to 3 regions.

1. Cut-off region :- The region below $I_E = 0$ mA is called cut-off region. In this both junctions are reverse biased.

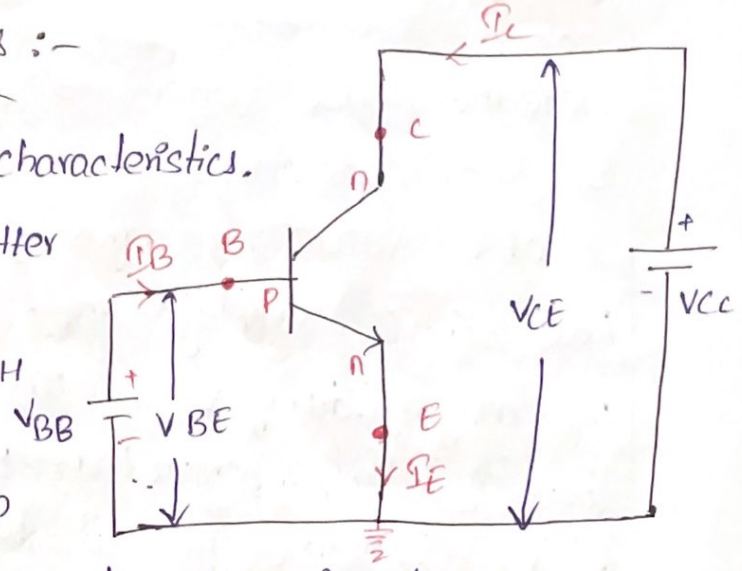
2. Active region :- The region between saturation & cut-off region is called active region.

3. saturation region :- The region to the left side of $V_{CB} = 0$ is called saturation region. Both junctions are in forward bias.

Common emitter configuration :- In this configuration, Base is input terminal, collector is output terminal, Emitter is common terminal.

Input characteristics :-

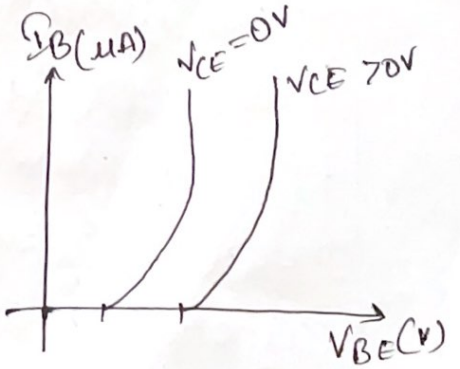
To determine I/P characteristics. the collector to emitter voltage is kept constant at zero volt and base current is increased from zero in equal steps by increasing V_{BE}.



The value of V_{BE} is noted for each setting of I_B.

This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B Vs V_{BE} are drawn.

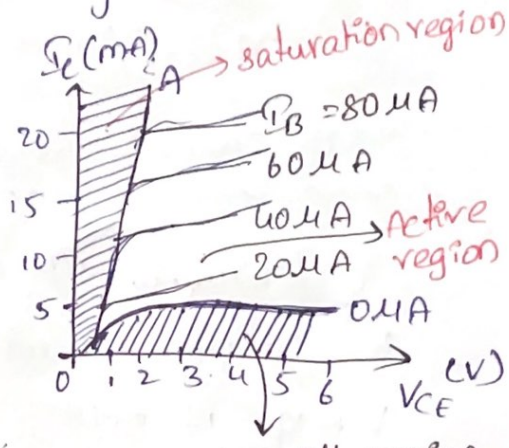
→ when $V_{CE}=0V$, the emitter base junction is forward biased and the junction behaves as a forward biased diode.



→ when V_{CE} increases, effective base width decreases that will decreases base current I_B. thats why the current shifts to the right as V_{CE} increased.

Output characteristics :-

Here the base current I_B is kept constant at a suitable value by adjusting base emitter voltage V_{BE}. The magnitude of V_{CE} is increased and I_C value is noted. Now the current of I_C Vs V_{CE} are plotted for different constant values of I_B.



The output characteristics have three regions. namely saturation region, cut-off region and active region.

→ In "saturation region" both junctions are forward biased and on increasing base current does not cause a corresponding large change in I_C. The ratio of V_{CE} to I_C in this region is called saturation resistance.

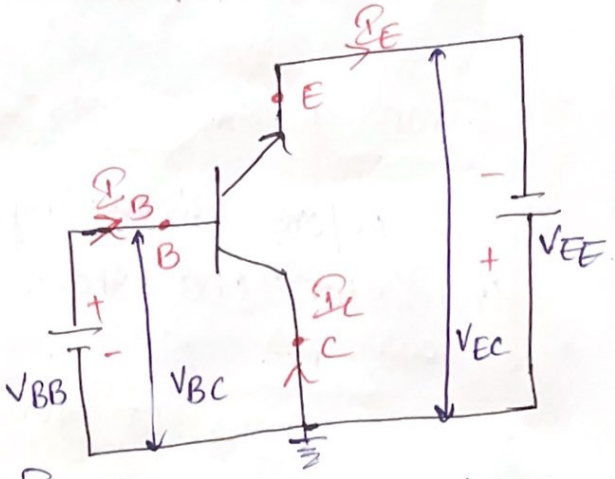
→ The region below the curve for $I_B = 0$ is called "cut-off region". In this region both junctions are reverse biased. In cutoff region transistor is said to be in off region. Hence I_C becomes almost zero and the collector voltage almost equals V_{CC};

→ In "active region" EB Junction is forward biased and the collector base junction is reverse biased, if the transistor is to be used as a linear amplifier, it should be operated in active region.

* CC configuration:-

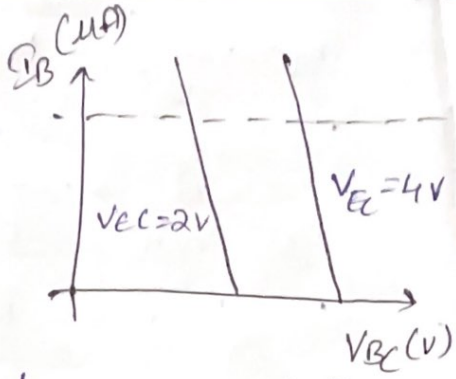
The V_{EC} is kept at a suitable fixed value.

The V_{BC} is increased in equal steps and corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} Vs I_B for different values of V_{EC} are drawn.

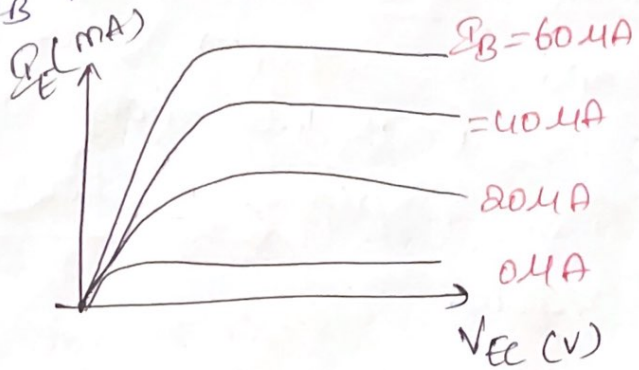


Output characteristics :-

The output characteristics are same as those of CE configuration.



→ It is the graph between output current I_E & output voltage V_{EC} at constant input current I_B.



* Transistor constants :-

The ratio of the variations in o/p to the variation in o/p current at constant output voltage is known as transistor constant or current amplification factor or forward current transfer ratio.

→ In a common-base configuration, the ratio of change in output current. ΔI_C to change in input current ΔI_E. when the collector to base bias voltage V_{CB} is maintained at

constant is called current amplification factor α

i.e $$\alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} = h_{fb}$$ (Interms of h-parameter)

In CB configuration, the collector current is slightly less than the emitter current, hence the α is slightly less than unity for commercial transistors, lies b/w 0.95 & 0.995

→ In common emitter configuration, the ratio of change in collector current ΔI_C to the change in base current when the collector to emitter voltage V_{CE} is constant, is known as the current amplification factor β.

$$\beta = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = h_{fe}$$

Since small changes in the base current produces a large changes in collector current, hence β value is always greater than unity. For commercial transistors β value lies between 20 and 500.

→ In common collector configuration, the ratio of change in emitter current I_E, to the change in Base current I_B when collector to Emitter voltage V_{CE} is constant. is known as current amplification factor γ

$$\gamma = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

* Relationship between $\alpha, \beta, \& \gamma$:-

we know that $\Delta I_E = \Delta I_C + \Delta I_B$

By defination $\Delta I_C = \alpha \Delta I_E$

$$\therefore \quad \Delta I_E = \alpha \Delta I_E + \Delta I_B$$

$$\Delta I_B = \Delta I_E (1-\alpha)$$

$$\Rightarrow \frac{\Delta I_B}{\Delta I_E} = \frac{\Delta I_E}{\Delta I_C}(1-\alpha)$$

$$\Rightarrow \frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha)$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \quad \text{or} \quad \boxed{\alpha = \frac{\beta}{1+\beta}} \quad \text{or}$$

$$\boxed{\frac{1}{\alpha} - \frac{1}{\beta} = 1}$$

it is clear that as 'α' approach unity, β approaches '∞' thas why CE configuration is used for almost all transistor applications, because of its high current gain 'β'.

We know that $\gamma = \frac{\Delta I_E}{\Delta I_B}$

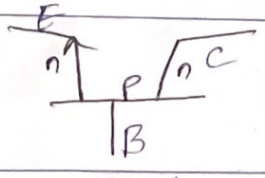
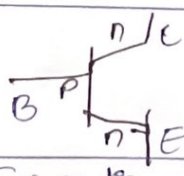
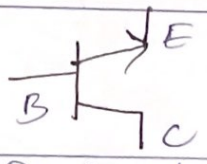
$$\Rightarrow \gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} \quad \left(\because \Delta I_E = \Delta I_B + \Delta I_C\right)$$

$$\Rightarrow \gamma = \frac{1}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

$$\Rightarrow \gamma = \frac{1}{1-\alpha}$$

$$\Rightarrow \boxed{\gamma = \frac{1}{1-\alpha} = (\beta + 1)}$$

Comparision of transistor configurations.

characteristics	CB	CE	CC
I/p voltage is applied b/w	E & B i.e V_{EB}	B & E i.e V_{BE}	B & C i.e V_{BC}
	C & B i.e V_{CB}	C & E i.e V_{CE}	E & C i.e V_{EC}
O/p voltage is taken b/w			
I/p current	I_E	I_B	I_B
O/p current	I_C	I_C	I_E
i/p Resistance	Low (about 100 Ω)	moderate (about 750 Ω)	High (about 750 KΩ)
O/p Resistance	Very high	high	low
current gain	$\alpha = I_C / I_E$	$\beta = I_C / I_B$	$\gamma = I_E / I_B$
voltage gain	About 150	About 500	less than 1
power gain	Medium	high	medium
phase shift b/w I/p & O/p voltage	In phase 0° or 360°	out of Phase 180°	In phase 0° or 180°
Symbol			
Applications.	For high frequency circuits	for audio frequency	for impedence matching.

→ Operating point

* BJT Biasing :- In order to operate transistor in the desired region an external dc voltage has to be applied with correct polarity and magnitude to the two junctions of the transistor. This is known as biasing of the transistor.

→ Because dc voltages are used to bias the transistor, biasing is known as dc biasing of the transistor.

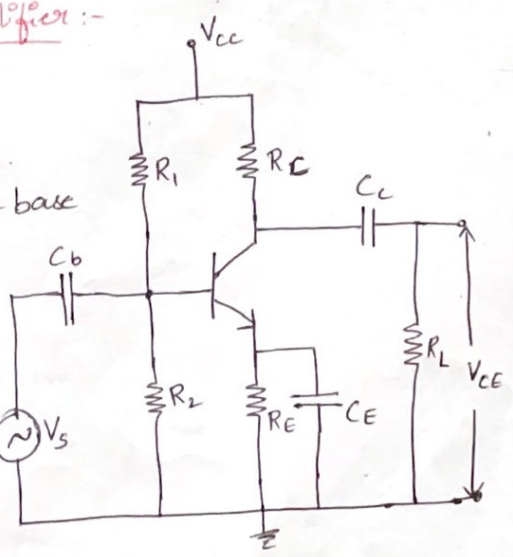
* Operating point :- When biasing is provided to a transistor, certain current and voltage conditions are established for the transistor.

→ These conditions are known as operating point or operating conditions or quiescent point (it means quite, still, inactive).

→ The operating point must be stable for proper operation of the transistor.

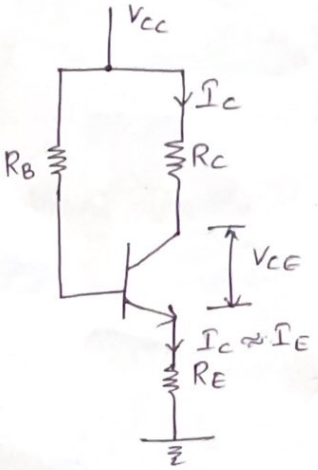
* DC equivalent model of CE amplifier :-

→ Transistor is biased with a common supply such that emitter-base junction is forward biased & collector-base junction is reverse biased, ie, transistor is in active region.



CE amplifier ckt.

→ In the absence of AC signal, the capacitors provide very high impedance ie, open circuit.



DC equivalent ckt.

→ Applying KVL to the collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

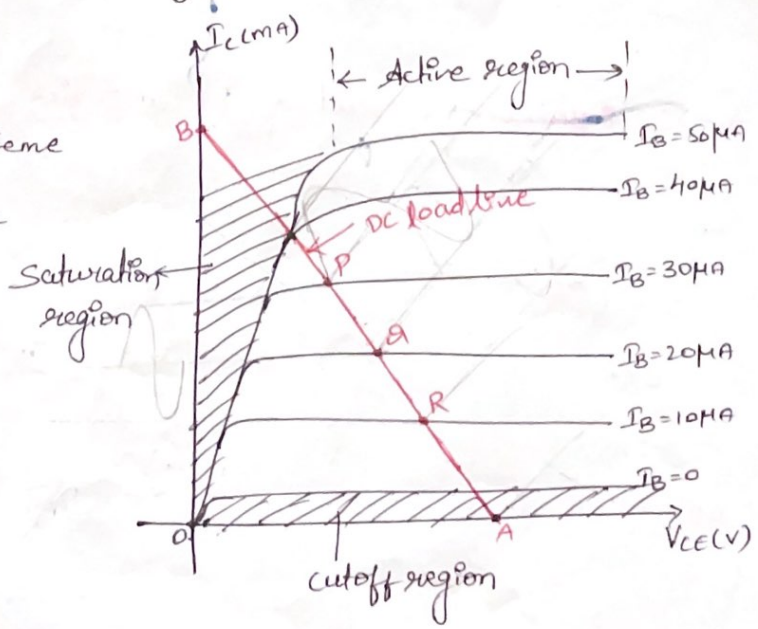
$$I_C (R_C + R_E) = V_{CC} - V_{CE}$$

$$\Rightarrow I_C = \left(\frac{-1}{R_C + R_E}\right) V_{CE} + \left(\frac{1}{R_C + R_E}\right) V_{CC}$$

$$I_C = \left(\frac{-1}{R_{dc}}\right) V_{CE} + \frac{V_{CC}}{R_{dc}} \qquad \because R_{dc} = R_C + R_E$$

→ Compare this equation with $y = mx + c$.

→ It is a straight line on the graph of I_C vs V_{CE} which is having slope $\left(\frac{-1}{R_{dc}}\right)$.



→ To determine the 2 extreme points on the line, assume

(i) $V_{CE} = V_{CC}$ & (ii) $V_{CE} = 0$

(i) When $V_{CE} = V_{CC}$

$\Rightarrow I_C = 0$, point A

(ii) When $V_{CE} = 0$

$\Rightarrow I_C = \frac{V_{CC}}{R_{dc}}$, point B

→ The line drawn between the points A & B on the output characteristics is called dc load line.

→ The 'dc' word indicates that only dc conditions are considered i.e., input ac signal is assumed to be zero.

→ The intersection of the characteristic curve and dc load line is the operating point.

→ The point is fixed on the curve, so it is called as quiescent point or Q-point.

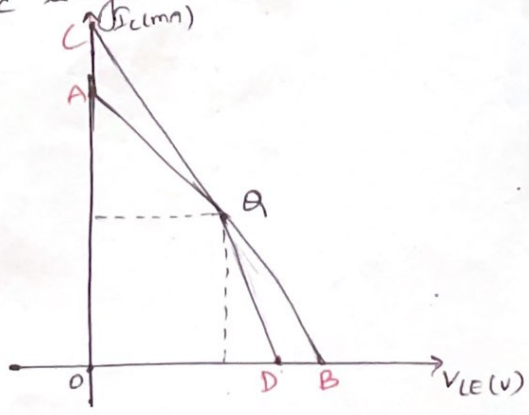
→ For different values of I_B, there will be different intersection points (P, Q, R in the fig.)

→ After choosing the Q point at the center of the dc load line, ac load line is also drawn through the Q point.

→ The effective ac load resistance Rac is given as

$$R_{ac} = R_C \| R_L$$

$$\text{slope of } CQD = \left(\frac{-1}{R_{ac}}\right)$$



→ To draw ac load line, max. V_{CE} & max I_C when the signal is applied are required.

max $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$, point D

max $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, point C

* Bias stabilization :-

→ The biasing circuit should be designed to fix the Q-point, but only fixing of the Q-point is not sufficient.

→ When designing the biasing circuit, care should be taken so that the Q-point will not shift into an undesirable region.

→ Three important factors are to considered while designing the biasing circuit which are responsible for shifting the Q-point.
(i) Temperature, (ii) Transistor current gain β, (iii) V_{BE}

* Thermal Runaway :- (I_{CO})

→ Minority carriers are temperature dependent. ie, they increase with the temperature.

→ The increase in the minority carriers increases the leakage current I_{CO}

→ Specifically, I_{CO} doubles for every 10°c rise in temperature.

→ Increase in I_{CO} in turn increases the I_C which leads to the shift of Q point.

→ This process will become cumulative leading to thermal runaway.

→ Due to this, the ratings of the transistor are exceeded which may destroy the transistor itself.

* Variation in V_{BE} :- V_{BE} is also temperature dependent. If Temp increases by 1°c then V_{BE} decreases by 2.5mV. This dependency of V_{BE} on temp. causes a change in I_B & hence I_C also changes.

* Current gain β :-

→ There are changes in the transistor parameters among different units of same type ie, if 2 transistors units of same type (same number, construction, parameters specified etc) are used in the circuit, there will be a change in β value in actual practice.

→ The β value may change from unit to unit, thus shifting the Q-point.

From all this explanation, the requirements of the biasing circuit can be summarised as follows:

* Requirements of a biasing circuit:

1) The emitter junction must be forward biased and the collector junction must be reverse biased, ie the transistor should be operated in the middle of the active region or Q-point should be fixed at the center of the active region.

2) The circuit design should provide a degree of temperature stability.

3) The Q-point should be made independent of the transistor parameters (β).

* Stability factor :-

→ In order to compare the stability provided by different biasing circuits, one term is raised called stability factor.

→ It indicates the degree of change in Q-point due to variation in temperature.

→ Since there are 3 variables (I_{CO}, V_{BE} & β) which are temperature dependent, 3 stability factors can be defined.

1) $$S = \frac{\partial I_C}{\partial I_{CO}}\bigg|_{V_{BE}, \beta \text{ constant}} \quad \text{or} \quad S = \frac{\Delta I_C}{\Delta I_{CO}}\bigg|_{V_{BE}, \beta \text{ constant}}$$

2) $$S' = \frac{\partial I_C}{\partial V_{BE}}\bigg|_{I_{CO}, \beta \text{ constant}} \quad \text{or} \quad S' = \frac{\Delta I_C}{\Delta V_{BE}}\bigg|_{I_{CO}, \beta \text{ constant}}$$

3) $$S'' = \frac{\partial I_C}{\partial \beta}\bigg|_{I_{CO}, V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \frac{\Delta I_C}{\Delta \beta}\bigg|_{I_{CO}, V_{BE} \text{ constant}}$$

Note: (i) Ideally, stability factor should be zero to keep Q-point stable.

(ii) Practically stability factor should have the value as minimum as possible.

$$\Delta I_C \simeq S \cdot \Delta I_{CO} + S' \Delta V_{EB} + S'' \Delta \beta$$

* Stability factor 'S' equation:-

→ For a CE configuration, I_C is given as:

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

differentiating this eqn w.r.to I_C,

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow (1-\beta) \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$\therefore \frac{\partial I_{CO}}{\partial I_C} = \frac{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}{1+\beta}$$

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

From the above eqn, it is clear that S should be as small as possible to have better thermal stability.

→ The process of making operating point independent of temperature changes (or) variations in the transistor parameters is known as stabilization.

→ For maintaining the Q-point independent of these variations the following techniques are used.

i) Biasing techniques, ii) Compensation techniques.

* Methods of transistor biasing :-

The most commonly used methods of transistor biasing are:

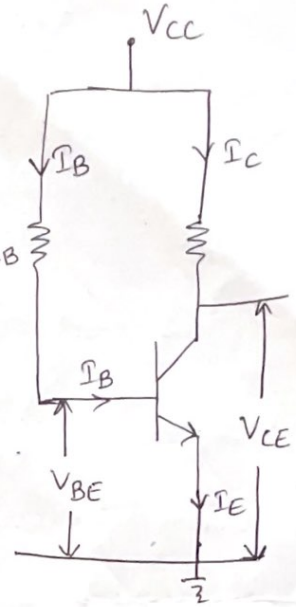
1) Fixed bias / Base resistor method
2) Emitter feedback bias
3) Collector to emitter feedback bias
4) Voltage divider bias or self bias or emitter bias.

1) Fixed Bias or Base bias method:

→ In this method a high resistance R_B is connected between the base and the V_{cc} supply.

→ Biasing is provided by V_{cc}

→ The required value of base current I_B can be made to flow by selecting the proper value of R_B



$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$V_{cc} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} \quad \text{— (1)}$$

→ V_{BE} is 0.3V for Germanium & 0.7V for Silicon (which is very small)

$$\Rightarrow I_B \cong \frac{V_{cc}}{R_B}$$

∴ V_{cc} & R_B are fixed, I_B will be fixed

→ So, the circuit is called Fixed Bias circuit.

→ In eqn. (1) β is not appearing & V_{cc}, R_B are fixed then the biasing point is also fixed.

Stability factor $S = \dfrac{1+\beta}{1-\beta \dfrac{dI_B}{dI_C}}$

→ But in fixed bias method, I_B is independent of I_C.

$$\text{so, } \frac{dI_B}{dI_C} = 0$$

$$\Rightarrow S = \frac{1+\beta}{1-\beta \times 0}$$

$$\Rightarrow S = 1+\beta$$

→ If $\beta = 100$, $S = 101$ which is very large i.e, fixed bias method has poor thermal stability.

* Advantages:

(i) The biasing circuit is very simple as only one resistance R_B is required.

(ii) Easy to fix the operating point anywhere in the active region by changing the value of R_B.

(iii) Provides maximum flexibility in design.

* Disadvantages:

(i) This method provides poor stabilization. It is because there is no means to stop a self increase in I_C due to temperature variations & individual variations.

(ii) Stability factor is very high. Therefore, there are strong chances of thermal runaway.

* Self bias or emitter bias or Voltage divider bias:-

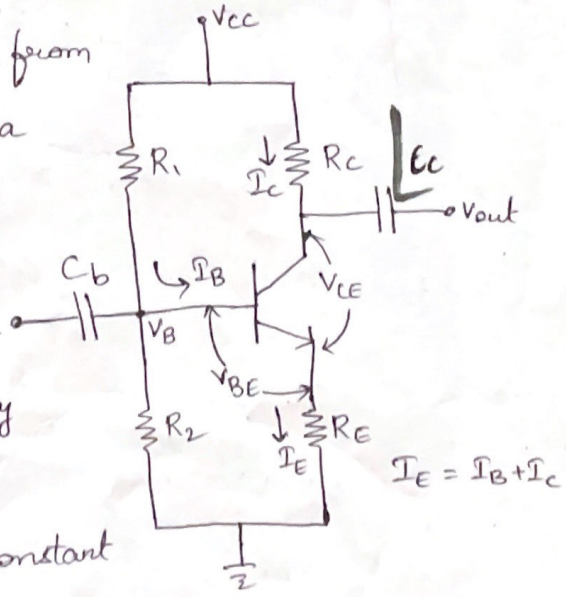
→ A simple circuit used to establish a stable operating point is the self bias configuration.

→ It is also known as universal bias stabilization ckt.

→ The name voltage divider is derived from the fact that resistors R_1 & R_2 form a potential divider across V_{cc}.

→ Voltage drop V_B across R_2 forward biases the emitter where as V_{cc} supply reverse biases the collector.

→ Self-bias circuit can be used as a constant current circuit.



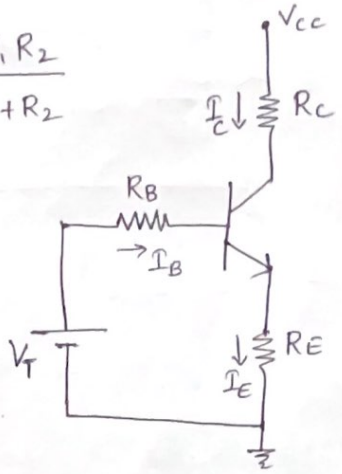
self bias circuit

→ If I_C ↑ses with ↑se in I_{CO} due to temperature, voltage drop across R_E ↑ses there by ↓ing I_B. So I_C is maintained almost constant.

Stability factor 'S':

→ By using Thevenins theorem self bias circuit can be modified as

$$V_T = \frac{R_2}{R_1+R_2} V_{CC} \quad \& \quad R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1+R_2}$$



Applying K.V.L

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$= I_B (R_B + R_E) + V_{BE} + I_C R_E$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_B + R_E} - \left(\frac{R_E}{R_B+R_E}\right) I_C$$

differentiate w.r.to I_C

[if T↑, I_{CO}↑, I_C↑, $\frac{I_C R_E}{R_B+R_E}$↑, I_B↓, I_C↓]

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B+R_E}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_E}{R_B+R_E}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$$

$$\therefore \boxed{S = (1+\beta)\cdot \frac{1+R_B/R_E}{1+\beta+R_B/R_E}}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

→ Ratio of R_B/R_E controls the value of stability factor S

if $\frac{R_B}{R_E} \ll 1$ then $S = \frac{(1+\beta)(1+0)}{(1+\beta)+0} = \frac{1+\beta}{1+\beta} = 1$

→ To improve the stability of self bias circuit, R_B must be choosen that

$$\boxed{R_B << R_E}$$

$$\frac{\partial I_C}{\partial V_{BE}} = S' = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$$\frac{\partial I_C}{\partial \beta} = S'' = \frac{S I_C}{\beta (1+\beta)}$$

* Compensation techniques :

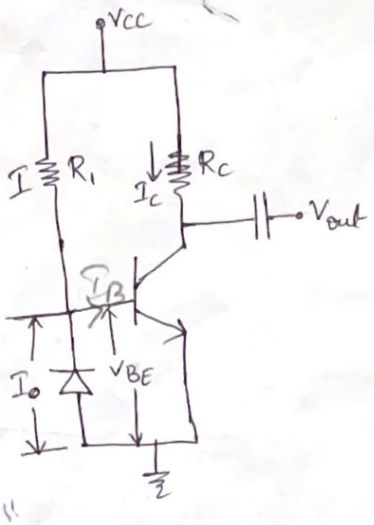
→ Compensation techniques use temperature sensitive devices such as diodes, transistors etc. to maintain operating point constant.

* Compensation against variation in I_{CO} :

→ Diode compensation techniques are commonly used for stabilizing transistors.

→ As shown in the circuit, diode is kept in reverse bias.

→ In reverse bias condition the current flowing through diode is only the leakage current (I_O).



→ If both diode & transistor are of same type & same material, then I_O ↑ses with temperature I_{CO} also ↑ses with the same rate.

$$I = \frac{V_{CC} - V_{BE}}{R_1} \quad \& \quad I = I_B + I_O$$

$$\Rightarrow I_B = I - I_O$$

as- $V_{BE} = 0.2V$

$$I \approx \frac{V_{CC}}{R_1}$$

$$I = I_B + I_O$$

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta (I - I_O) + (1+\beta) I_{CO}$$

$$I_C = \beta I - \beta I_O + \beta I_{CO} \quad (\because \beta >> 1)$$

$$\Rightarrow I_C = \beta I \quad (\because I_O \approx I_{CO})$$

as I is constant, I_C remains fairly constant

* Thermistor compensation:

→ Thermistor is having negative temperature coefficient. Its resistance ↓ses expotentially with increasing temperature.

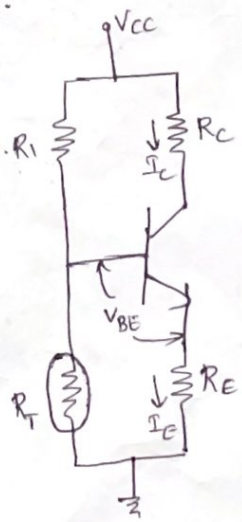
→ R_T is the thermistor, with ↑se in temp. R_T ↓ses. Hence voltage drop also ↓ses (i.e, base voltage).

→ So, V_{BE} ↓ses which reduces I_B.

→ This behavior will tend to offset the ↑se in I_C

$$I_C = \beta I_B + (1+\beta) I_{CO} \uparrow$$

↓ constant



* Transistor at low frequencies:

→ The cutoff frequencies of single stage BJT/FET amplifiers are influenced by the RC combinations formed by the network capacitors C_E, C_C etc. and the resistive parameters present in the network.

→ C_C is the coupling capacitor, it couples the output of the amplifier to the load or to the next stage. It blocks dc and passes only ac part of the amplified signal.

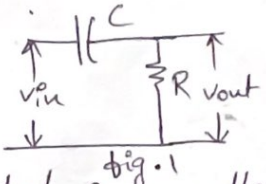


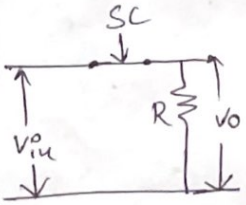
fig. 1

→ C_E is Emitter by pass capacitor, it is connected in parallel with R_E to provide a low reactance path to the amplified a.c signal.

$$\text{Capacitive reactance } X_C = \frac{1}{2\pi f C}$$

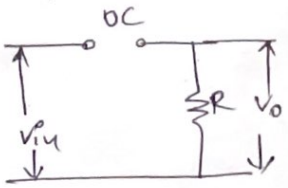
→ At very high frequencies, capacitor acts as short circuit.

$$X_C = \frac{1}{2\pi f C} \cong 0 \; ; \; X_C = 0$$



→ At very low frequencies, capacitor acts as open circuit

$$X_C = \frac{1}{2\pi f C} = \frac{1}{0} = \infty \; ; \; X_C = \infty$$



Applying voltage divider rule for fig. 1

$$V_{out} = \frac{R V_{in}}{R - jX_C}$$

magnitude of V_{out} is given as

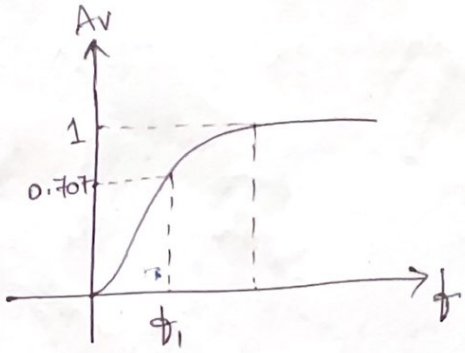
$$|V_{out}| = \frac{R V_{in}}{\sqrt{R^2 + X_C^2}}$$

Assume $X_C = R$

$$\Rightarrow |V_{out}| = \frac{R V_{in}}{\sqrt{R^2 + R^2}}$$

$$|V_{out}| = \frac{V_{in}}{\sqrt{2}}$$

$$|A_V| = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{2}}$$



$A_V = 0.707$ at $X_C = R$

Now, as per assumption

$X_C = R$

$$\frac{1}{2\pi f_1 C} = R$$

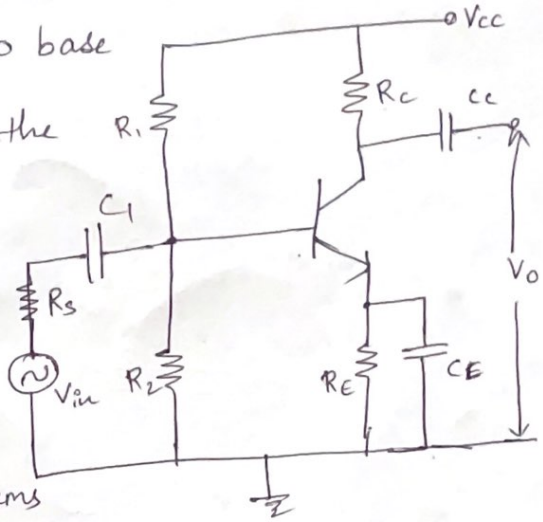
$$\boxed{f_1 = \frac{1}{2\pi RC}}$$

f_1 — lower cutoff frequency

* CE amplifier :

→ An amplifier that is formed using a CE configured transistor is called as CE amplifier.

→ As shown in fig. i/p is given to base terminal and o/p is taken from the collector terminal.



Working of CE amplifier :

→ Biasing circuit / voltage divider :

The resistances R_1, R_2, R_E forms the voltage biasing and stabilization circuit

→ C_{in} is used to couple the signal to the base terminal of the BJT

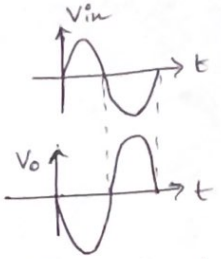
→ C_E, emitter bypass capacitor is used parallel with R_E to provide a low reactance path to the amplified AC signal. If C_E is not present, R_E will cause a voltage drop, thereby ↓sing o/p voltage.

→ C_C is the coupling capacitor which couples one stage of amplification to the next stage. This is used to isolate the DC bias settings of the two coupled circuits.

→ Operation of CE amplifier:

→ As the input voltage V_{in} ↑ses, the base current I_B also ↑ses, which inturn ↑ses I_C.

→ This causes ↑se in the voltage drop across the R_C, which results in a ↓sed o/p voltage V_o



$$V_o = V_{cc} - I_C R_C$$

→ Similarly, as the i/p voltage goes on decreasing I_B & I_C ↓se, due to which the voltage drop across R_C also ↓ses thereby ↑sing V_o.

→ This indicates that for +ve half cycle there is a amplified negative half cycle at the o/p & for -ve half cycle, o/p is amplified +ve half cycle.

→ Hence there exists a phase shift of 180° b/w i/p & o/p waveforms of the CE amplifier for which it is also referred as Inverting amplifier.

$$\text{Current gain } \beta = \frac{\Delta I_C}{\Delta I_b}$$

$$\text{Voltage gain } A_V = \beta \frac{R_C}{R_b}$$

→ Adv CE amplifier has high gain compared to other amplifiers, hence this is mostly used in audio amplifiers.

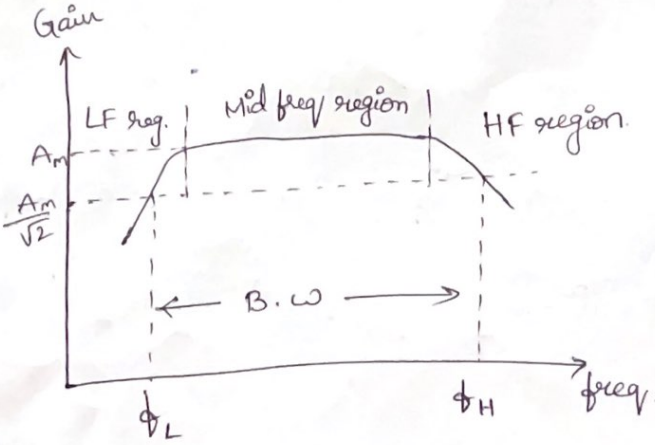
→ CE amplifier frequency response:

→ The voltage gain of a CE amplifier varies with signal frequency,

→ this is because the reactance of the capacitor in the circuit changes with signal frequency and hence affects the V_o.

→ The curve drawn between voltage gain & signal frequency is known as frequency response.

$$X_C = \frac{1}{2\pi f C}$$



→ At LF ($<f_L$), the X_C is relatively high & hence very small part of the signal will pass from the amplifier stage to load.

→ At HF ($>f_H$), X_C is very small & it behaves as short circuit. This ↑ses the loading effect of the amplifier stage & serves to reduce A_V.

→ At mid frequencies (f_L to f_h), the A_V is constant. ∈ The effect of C_c is such as to maintain a constant A_V. Thus, as the frequency ↑ses in this range, X_c of C_c ↓ses, which tends to ↑se the gain.

→ Bandwidth is the difference between the upper and lower frequencies in a continuous band of frequencies

$$B.\omega = f_H - f_L$$

* Gain Bandwidth product:

→ The gain bandwidth product of an amplifier is the product of the amplifier's bandwidth & the gain at which the bandwidth is measured.

→ f_H & f_L are called as cutoff or corner frequency points, indicates the frequencies at which the power associated with the o/p falls to half of its maximum value (A_m)

→ $A_m \frac{A_m \times 1}{\sqrt{2}} = 0.707 \overset{\wedge}{}$ of A_m or 3dB point is considered as the gain at which the cut off frequencies occur.

G_I = Gain , BW = Bandwidth

$$G_I \times BW = A_i \times BW \text{ or } G_I \times BW = A_V \times BW$$

$$BW = f_H - f_L \approx f_H$$

$$G_I \times BW = A_i \times f_H$$

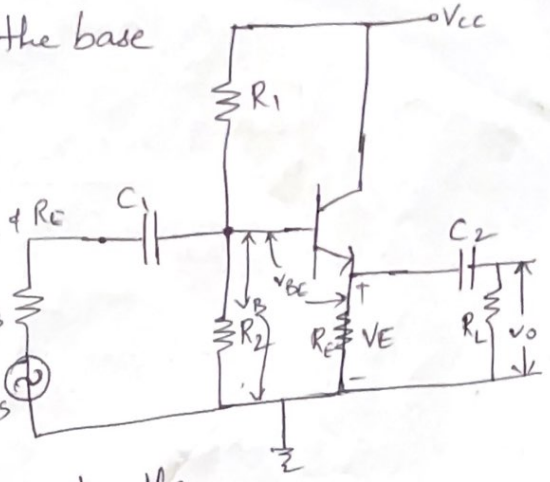
$$\boxed{G_I \times BW = \frac{A_i}{2\pi RC}} \quad \left[\because f = \frac{1}{2\pi RC}\right]$$

* Emitter follower (or) CC amplifier:

→ In CC amplifier i/p is given at the base & o/p is taken from collector.

→ DC biasing is provided by R_1, R_2 & R_E

→ R_L is capacitor coupled to the emitter terminal of the transistor



→ When a signal is applied via C_1 to the base, V_B is ↑sed & ↓sed as the signal goes +ve & -ve respectively.

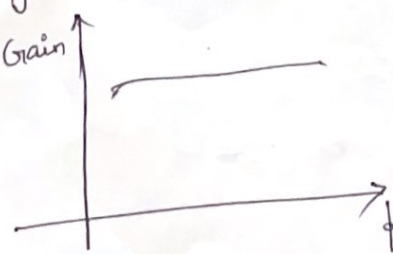
→ From the circuit $V_B = V_{BE} + V_E \Rightarrow V_E = V_B - V_{BE}$

→ considering V_{BE} constant, variation in V_B appears at emitter & V_E will vary same as V_B.

→ Since, emitter is o/p terminal it can be noted that the o/p voltage is the same as & i/p voltage.

→ CC circuit emitter terminal follows the signal voltage applied to the base. Hence CC amplifier is also known as Emitter follower.

* Frequency response of CC amplifier



→ Voltage Gain is low in CC

* Multistage amplifiers:

→ A transistor circuit containing more than one stage of amplifier is known as multistage amplifier.

→ The o/p of a single stage amplifier is usually not sufficient.

→ In multistage amplifiers, the o/p of 1st stage is coupled to the i/p of next stage using a coupling device.

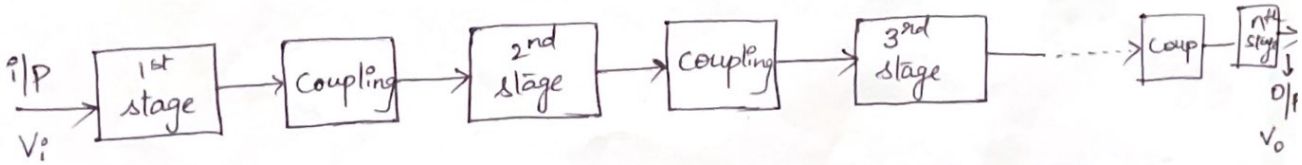
→ This process of joining 2 amplifier stages using a coupling device can be called as cascading.

→ The purpose of coupling device is

(i) To transfer ac o/p of one stage to the i/p of next stage.

(ii) To isolate the dc conditions of one stage from next stage.

(iii) To reduce or eliminate the loading effect

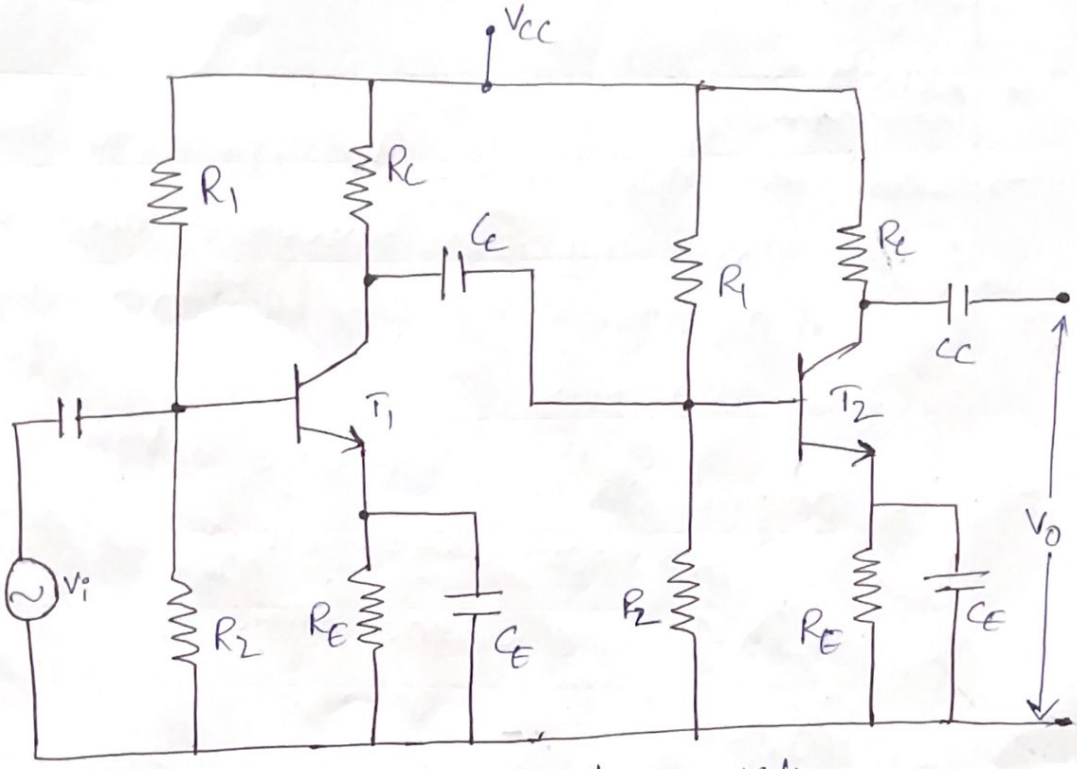


Overall Voltage gain $A_{Vt} = A_{V_1} \times A_{V_2} \times A_{V_3} \cdots \times A_{V_n}$

$$= \frac{V_2}{V_i} \times \frac{V_3}{V_2} \times \frac{V_4}{V_3} \cdots \times \frac{V_o}{V_n}$$

$$\boxed{A_{Vt} = \frac{V_o}{V_i}}$$

* Rc coupled Amplifier :- (Two cascade CE Amp)



2 stage : Rc coupled Amplifier.

As shown in the figure, the first stage is connected to the second stage through the coupling capacitor C_c and resistor R_c. Therefore this amplifier is called as Rc coupled amplifier.

→ The resistors R_1, R_2 form the self bias & R_E form stabilization network.

→ The emitter bypass capacitor offers low reactance path to the signal. This method of

coupling is widely used in cascade amplifier stages.

* Working:-

→ when the input voltage V_i applied to the base of the first transistor through a input capacitor C_{in}, it appears in the amplified form across its collector load R_c.

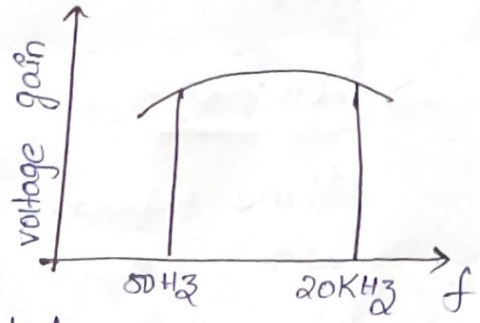
→ The output of the first stage is given to the base of the next stage through coupling capacitor C_c. The second stage does further amplification of the signal.

→ The coupling capacitor here, helps in blocking the flow of d.c. components from first stage to the second stage. Thus the biasing of the second stage will not disturbed.

→ The output signal is the twice amplified replica of the input signal. The output signal is in phase with the input signal because it has been reversed twice.

Frequency response of RC coupled amplifier:-

→ Frequency response of RC coupled amplifier is uniform over mid frequency range of 50Hz to 20KHz.



→ The voltage gain drops off at low <50Hz & high >20KHz frequencies

i) At low frequencies (<50Hz), the reactance of coupling capacitor "C_c" is quite high and hence very small part of signal will pass from one stage to the next stage. & voltage gain falls at low frequencies.

ii) At high frequencies (>20KHz), the reactance C_c is very small & it behaves as short circuit. This increases the loading effect of next stage & serves to reduce the voltage gain.

∴ voltage gain falls at high frequencies.

→iii) At mid frequencies (50Hz to 20KHz), the voltage gain of the amplifier is constant. The effect of coupling capacitor in this frequency

range is such so as to maintain a uniform voltage gain.

→ Advantages :-

1) The frequency response is excellent.
2) This circuit is very compact & extremely light
3) cost is low because it employs resistors & capacitors which are cheap.

* Disadvantages :-

1. low voltage & power gain
2. They have the tendency to become noisy
3. Impedence matching is poor.

Applications :-

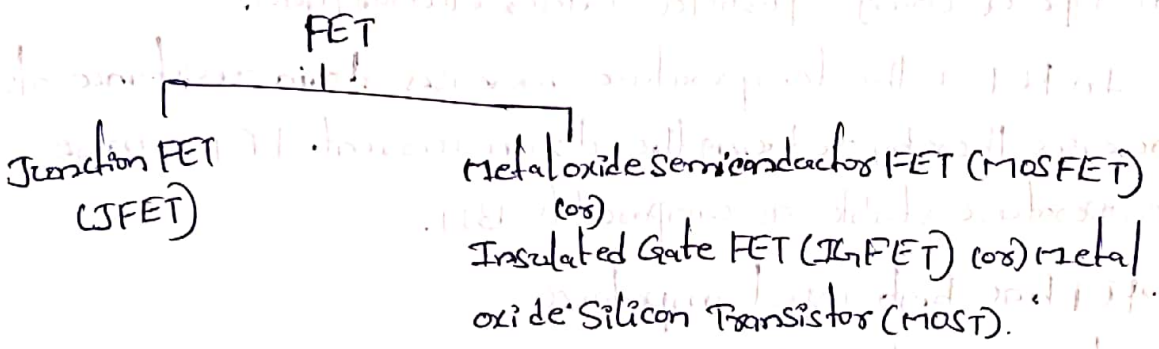
1. widely used as voltage amplifier
2. They have excellent audio fidelity over a wide range of frequency
3. Due to poor impedence matching, Rc coupli is rarely used in the final stages.

FET (Field Effect Transistor):-

The FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name Field Effect Transistor (FET).

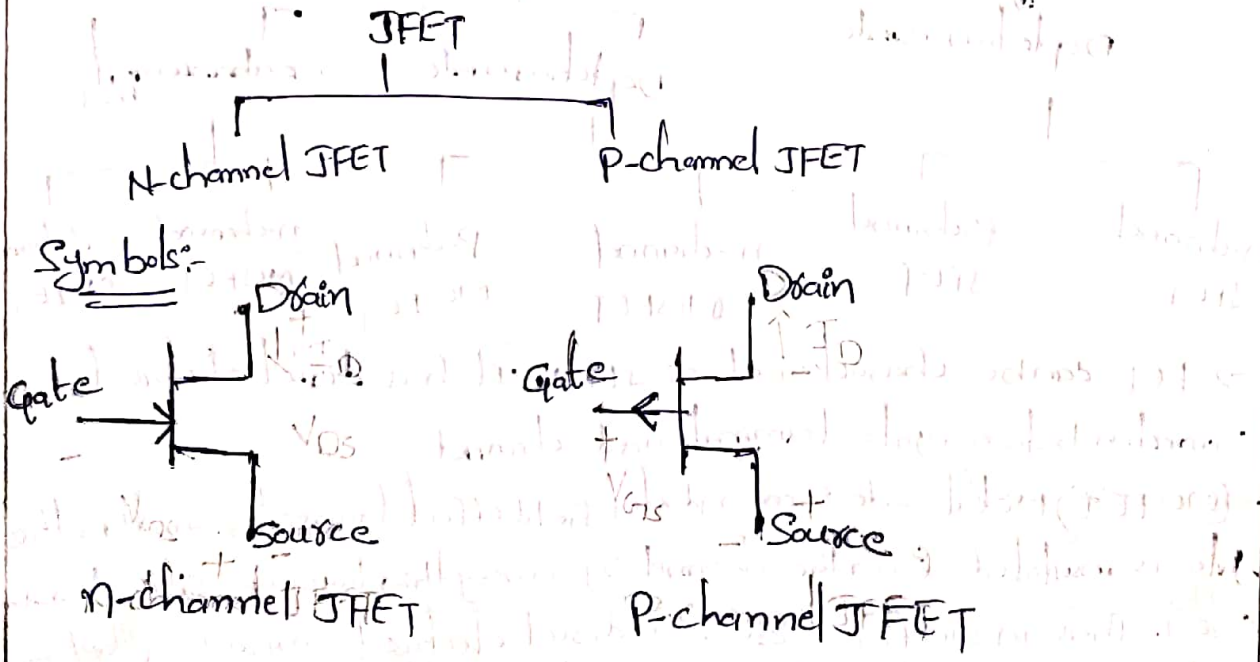
→ As current conduction is only by majority carriers, FET is said to be a unipolar device.

→ Based on the construction, the FET can be classified into 2 types.



→ Depending upon the majority carriers, JFET has been classified into 2 types, namely ① N-channel JFET with electrons as the majority carriers

② P-channel JFET with holes as the majority carriers.



Features of FET:-

→ FET is a voltage control device because the voltage applied between the gate and source(V_{GS}) controls the drain current(I_D).

→ The name field effect is derived from the output current I_{DSS} is controlled by an electric field; setup between gate and source terminals.

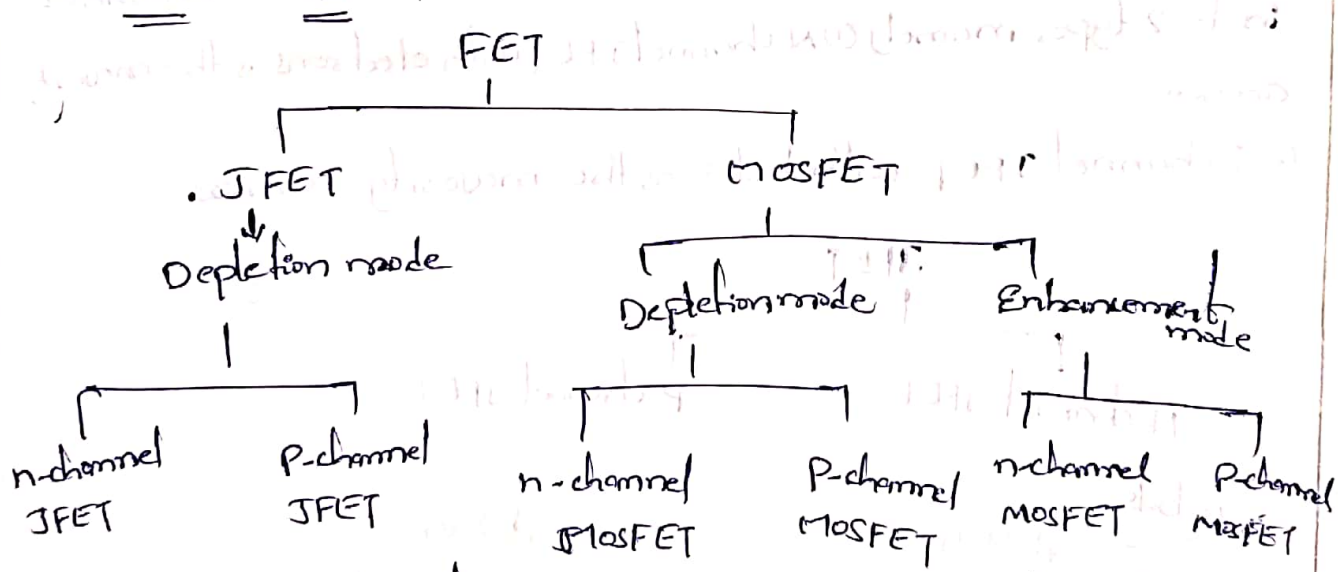
→ FET is a unipolar device because current is carried by only one type of charge particles either electrons/holes.

→ In FET as the temperature increases drain resistance also increases thereby reducing the drain current. FET is more temperature stable as compared to BJT.

→ FET has high input impedance

→ It requires less space.

Classification of FET



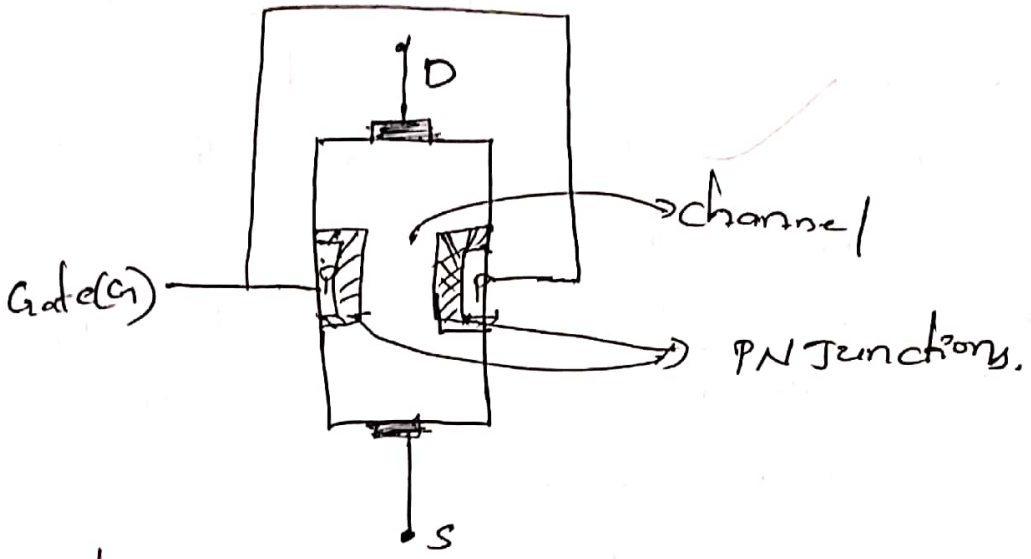
→ FET can be characterised as JFET. It has direct electrical connection between gate terminal and channel.

→ (MOSFET) Metal oxide semiconductor field effect transistor. In this the gate is insulated from the channel by a very thin layer of silicon dioxide (SiO_2). Thus in MOSFET there is a direct electrical connection between gate terminal & channel.

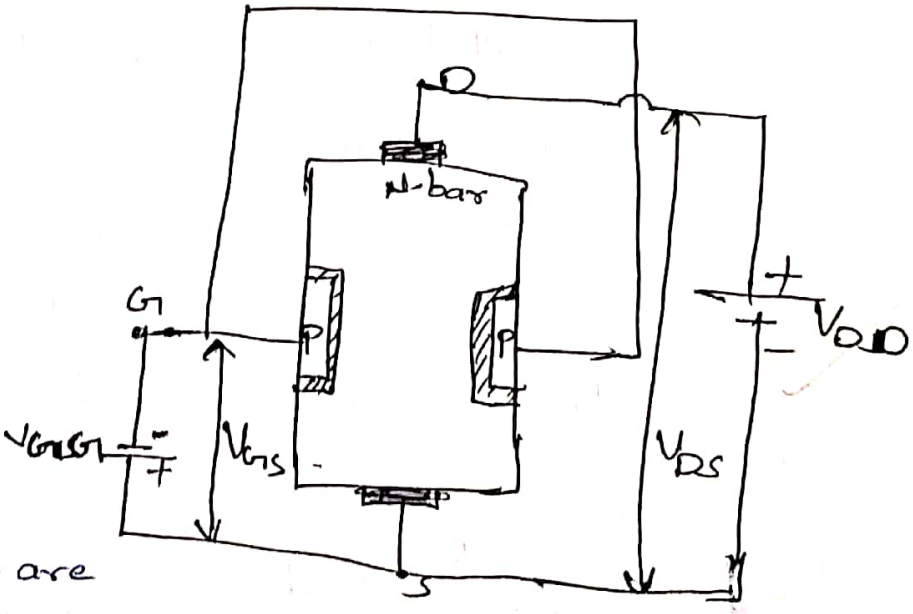
WIMP

Construction of N-channel JFET:-

N-channel JFET consists of N-type bar which is made up of silicon. ohmic contacts (terminals), made at the two ends of the bar, are called source and drain. The N-type bar is diffused with P-type impurities on two opposite sides and connected together and that can be taken as a "gate" terminal. Then two PN junctions are formed.



Operation:-



Source:-(S)

This terminal is connected to negative Pole of the battery.

Electrons which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D):- This terminal is connected to the positive terminal of the battery. The majority carriers leave the bar through this terminal.

Gate (G):- Always Gate is connected in reverse bias

channel:- The region between the two depletion regions is called the channel.

→ When $V_{GS}=0$ & $V_{DS}=0$, i.e., when no voltage is applied between drain & source and gate & source, the thickness of the depletion regions around the PN junction is uniform.

→ When $V_{DS}=0$ & V_{GS} is decreased from '0', the PN junctions are reverse biased & hence the thickness of the depletion region increases, and finally channel will disappear and two PN junctions are contact with each other.

In this condition channel is said to be in cutoff region.

→ "The value of the V_{GS} which is required to cutoff the channel is called the "cutoff voltage V_c".

→ When $V_{GS}=0$ & V_{DS} is increased from zero, the positive terminal attracts majority charge carriers (electrons) & low through the N-channel from source to drain so current I_D flows from drain to source.

$$I_D = \frac{A V_{DS}}{\rho L}$$

L = length of channel, V_{DS} = Drain to Source Voltage

A = ~~Cross~~ area of channel.

ρ = resistivity of the channel

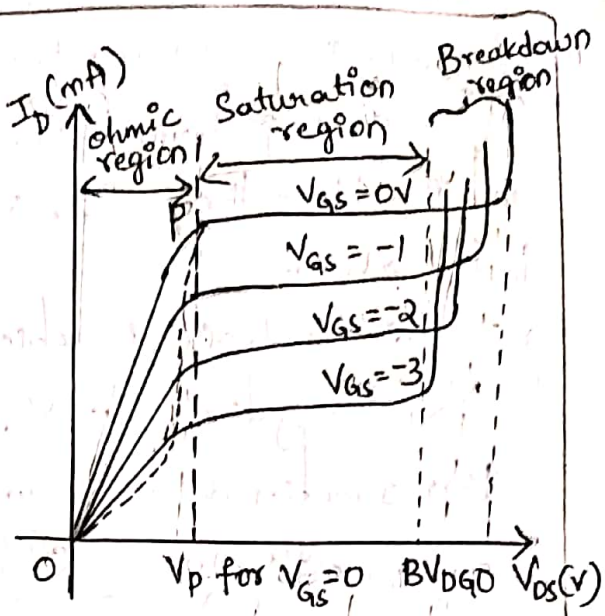
V-I characteristics of N-channel JFET

Drain characteristics:-

1) Drain characteristics are drawn between Drain to source voltage (V_{DS}) & Drain current (I_D) by keeping V_{GS} constant.

→ As V_{DS} increases, I_D increases and as V_{GS} increases I_D decreases.

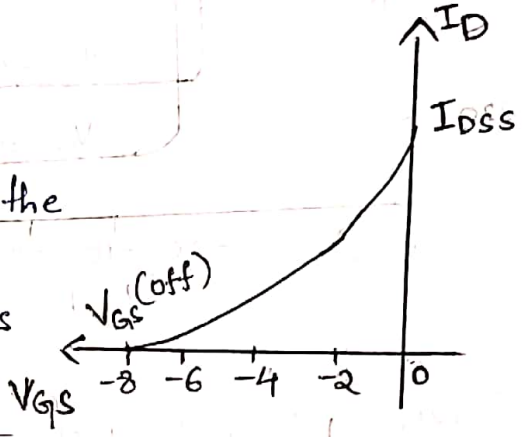
→ When $V_{DS} = V_P$, I_D becomes maximum, when V_{DS} is increased beyond V_P, the length of saturation region increases. Hence there is no further increase of "I_D".



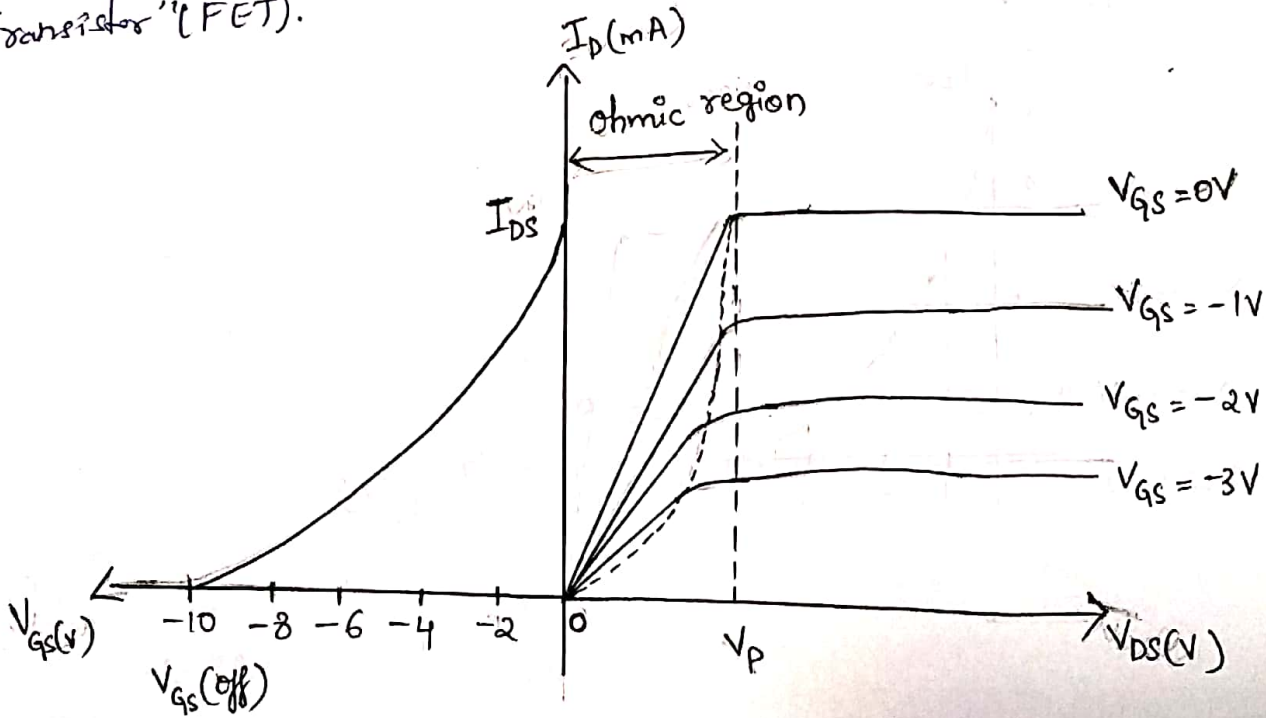
Drain Characteristics

Transfer Characteristics:-

Transfer characteristics are drawn between V_{GS} and I_D. As V_{GS} decreases the drain current decreases and finally becomes zero i.e., the drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage is applied to the gate. Hence the device has been given the name "Field Effect Transistor" (FET).



Transfer Characteristics.



Characteristic Parameters of JFET:- In JFET, the drain current "I_D" depends on the drain voltage V_{DS} & the gate voltage V_{GS}.

① **mutual conductance (or) Transconductance (g_m):-** It is the slope of the transfer characteristics curves & is defined by

$$g_m = \left(\partial I_D / \partial V_{GS}\right)_{V_{DS}=K}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at constant drain voltage.

② **Drain resistance (r_d):-** It is the reciprocal of the slope of the drain characteristics & is defined by $r_d = \frac{\partial V_{DS}}{\partial I_D} \Big|_{V_{GS}=\text{constant}}$

i.e., ratio of small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage.

③ **Amplification factor (μ):-** It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current.

$$\mu = \left(-\partial V_{DS} / \partial V_{GS}\right) \Big|_{I_D=\text{constant}}$$

→ Relationship between g_m, r_d & μ is given by

$$\boxed{\mu = g_m r_d}$$

Comparision of BJT & JFET :-

BJT	JFET
→ Current control device	→ Voltage control device
→ It is a bipolar device. The conduction level is a function of 2 types of charge carriers electrons and holes	→ It is a unipolar device. The conduction is only on electrons in n-channel JFET and holes in P-channel JFET.
→ It has low input resistance	→ It has high input resistance typically mega ohms
→ It has much higher sensitivity to changes in the applied signal	→ It has less sensitivity to changes in the applied signal.
→ It has high AC Voltage gain	→ It has low AC Voltage gain
→ It is a very sensitive to temperature variation	→ It is more temperature stable and more easily integrated on circuits.
→ occupies more space than JFET	→ occupies less space than BJTs.

Applications of FET :- (1) Used as Buffer
(2) Used as RF amplifiers
(3) as voltage variable resistor
(4) used in oscillator circuits.

UNIT-III

1) When a reverse gate voltage of 12V is applied to JFET, the gate current is 1nA. Determine the resistance between gate and source?

Soln:- Given $V_{GS} = 12V$, $I_G = 10^{-9}A$ $(\because 1nA = 10^{-9}A)$.

$\therefore$ Gate-to-source resistance $= \frac{V_{GS}}{I_G} = \frac{12}{10^{-9}} = 12$~~,000MΩ~~

$= 12,000 M\Omega$

---

2) When the reverse gate voltage of JFET changes from 4 to 3.9V, the drain current changes from 1.3 to 1.6mA. Find the value of transconductance?

Soln:- $\Delta V_{GS} = 4 - 3.9 = 0.1V$

$\Delta I_D = 1.6 - 1.3 = 0.3mA$

$\therefore$ Transconductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3}}{0.1} = 3m$ mho

---

3) A FET has a drain current of 4mA. If $I_{DSS} = 8mA$ and $V_{GS(off)} = -6V$. Find the values of V_{GS} and V_P.

Soln:- Given data $V_{GS(off)} = -6V$, $I_{DSS} = 8mA$, $I_D = 4mA$

$V_{GS} = ?$, $V_P = ?$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$4 \times 10^{-3} = 8 \times 10^{-3}\left(1 - \frac{V_{GS}}{(-6)}\right)^2$$

$$4 = 8\left(1 + V_{GS}/6\right)^2 \quad ; \quad \sqrt{4/8} = 1 + \frac{V_{GS}}{6}$$

$$\frac{1}{\sqrt{2}} = 1 + \frac{V_{GS}}{6}$$

$$\therefore \boxed{V_{GS} = -1.76V}$$

$$V_p = |V_{GS(off)}|$$

$$\boxed{V_p = 6V}$$

4) An N-channel JFET has $I_{DSS} = 8mA$ and $V_p = -5V$. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for $V_{GS} = -2V$ in the pinch-off region.

Soln:- Given data

$$I_{DSS} = 8mA, \quad V_p = -5V$$

The minimum value of V_{DS} for pinch-off to occur for $V_{GS} = -2V$

$$V_{DS\,min} = ?, \quad I_{DS} = ?$$

$$V_{DSmin} = V_{GS} - V_p$$

$$= -2 - (-5) = 3V$$

$$\boxed{V_{DSmin} = 3V}$$

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$= 8 \times 10^{-3}\left(1 - (-2)/(-5)\right)^2 = 2.88mA$$

$$\boxed{\therefore I_{DS} = 2.88mA}$$

(5) For a N channel JFET, $I_{DSS} = 8.7mA$, $V_P = -3\,V$, $V_{GS} = -1V$.
Find the values of ① I_D ② g_{mo} ③ g_m

Soln: Given data

$I_{DSS} = 8.7mA$, $V_P = -3V$, $V_{GS} = -1V$

$I_D = ?$ $g_{mo} = ?$ $g_m = ?$

① $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 8.7 \times 10^{-3}\left(1 - \frac{(-1)}{(-3)}\right)^2$

$= 8.7 \times 10^{-3}\left(\frac{2}{3}\right)^2$

$I_D = 3.87\,mA$

② $g_{mo} = \frac{-2I_{DSS}}{V_P} = \frac{-2 \times 8.7}{-3} = 5.8mS$ (or) $5.8\,mA/V$

③ $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$

$= 5.8\left(1 - \frac{-1}{-3}\right)$

$g_m = 3.87mS$

(6) An N-channel JFET has $I_{DSS} = 10mA$ & $V_P = -5V$. If $I_D = 2.5mA$, Find the value of V_{GS} & $V_{DS(sat)}$.

Soln: Given data $I_{DSS} = 10mA$, $V_P = -5$, $I_D = 2.5mA$

$V_{GS} = ?$, $V_{DS(sat)} = ?$

we know that $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$

$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = -5\left(1 - \sqrt{\frac{2.5}{10}}\right) = 2.5V$

$V_{DS(sat)} = V_{GS} - V_P = -2.5 - (-5) = 2.5V$

(7) A JFET has a pinch-off voltage of -4V & the saturation current of 8mA. Find the drain current if $V_{GS} = -3V$.

given data $V_P = -4$, $V_{GS} = -3$, $I_{DSS} = 8mA$, $I_D = ?$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8 \times 10^{-3}\left(1 - \frac{(-3)}{(-4)}\right)^2$$

$$I_D = 0.5mA$$

MOSFET (metal oxide semiconductor Field Effect Transistor)

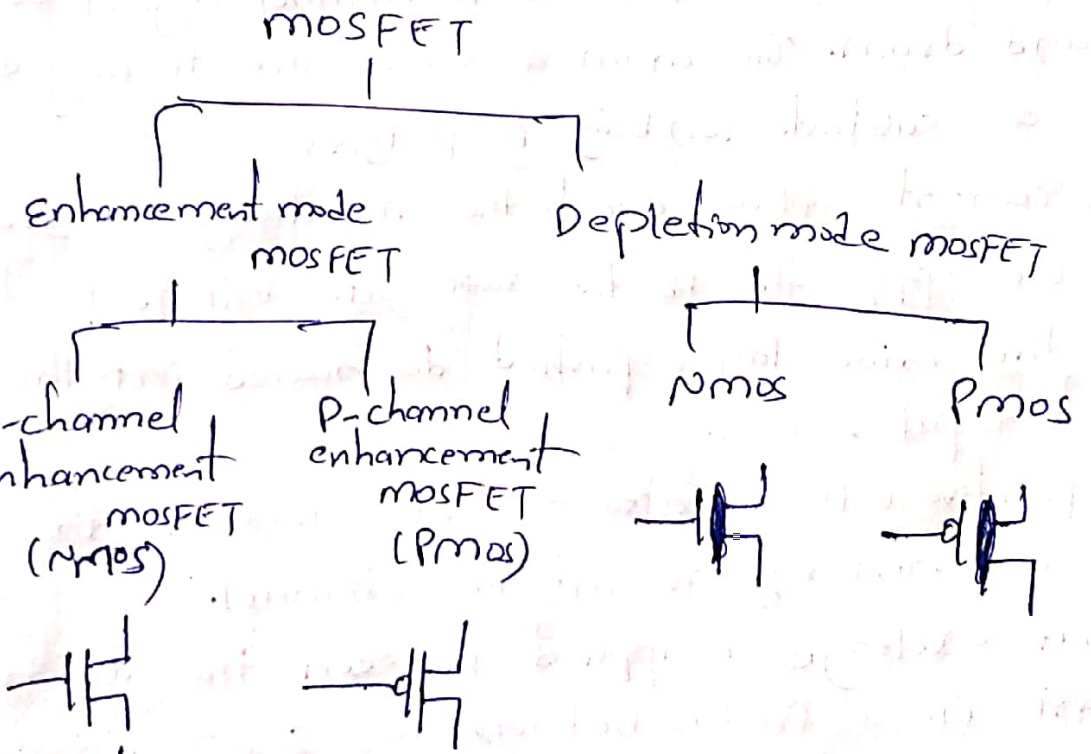
→ The MOSFET transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices.

→ The MOSFET is 4 terminal device with Source (S), Gate(G), Drain (D) and Body (B) terminals.

→ The body of the MOSFET is frequently connected to the source terminals so making it a 3 terminal device like field effect transistor.

The MOSFET can function in 2 ways ① Enhancement mode ② Depletion mode

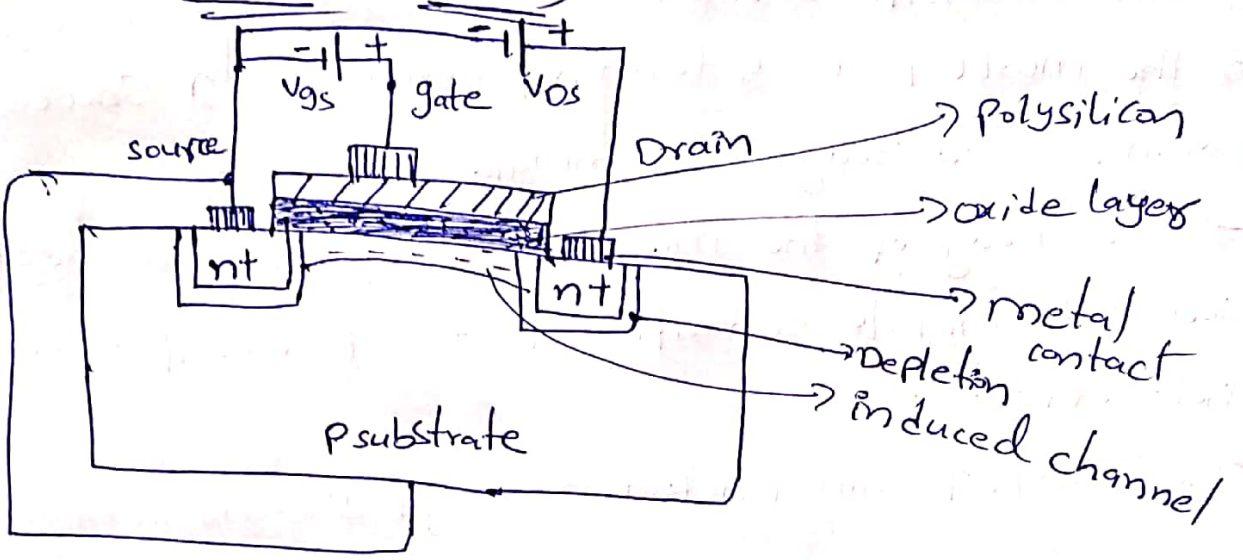
MOSFET classification



Enhancement mode :- when there is no voltage on the gate the device doesnot conduct. more is the voltage on the gate, the better the device can conduct.

Depletion mode:- when there is no voltage on the gate, the channel shows its maximum conductance. As the voltage on the gate is either positive (or) negative, the channel conductivity decreases.

Nmos (enhancement mode)



→ The nchannel mosFET has a N-channel region between Source and drain. The drain & source are heavily doped n+ regions & substrate (or) body is P-type.

→ The current flow due to the negatively charged electrons. when we apply the positive gate voltage the holes present under the oxide layer pushed downward into the substrate with a repulsive force.

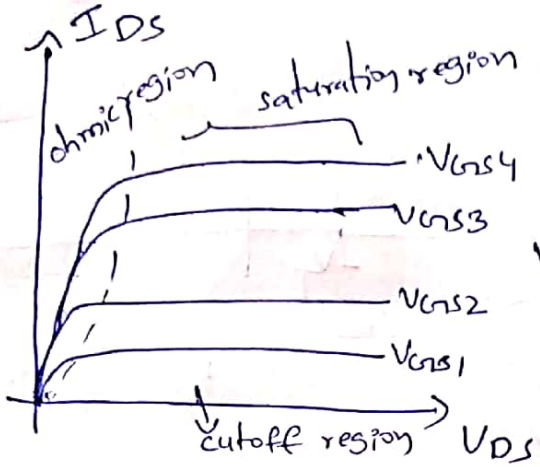
→ The positive voltage also attracts electrons from the n+ source & drain regions into the channel.

→ Now, if a voltage is applied between the drain & source the current flows freely between the source & drain & the gate voltage controls the electrons in the channel.

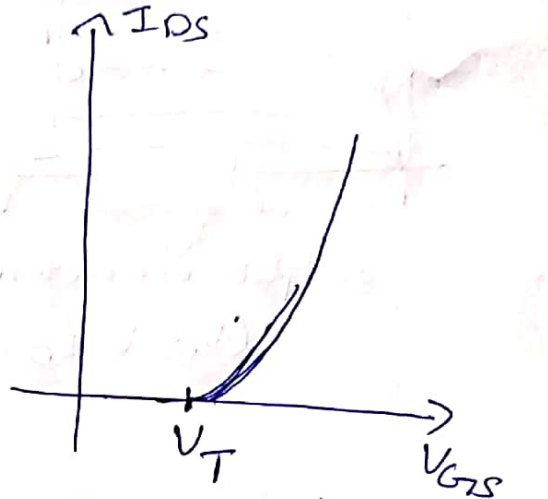
→ output characteristics (V_{DS} Vs I_D where V_{GS} = constant)

→ Transfer characteristics (V_{GS} Vs I_D)

I-V Characteristics of NMOS enhancement



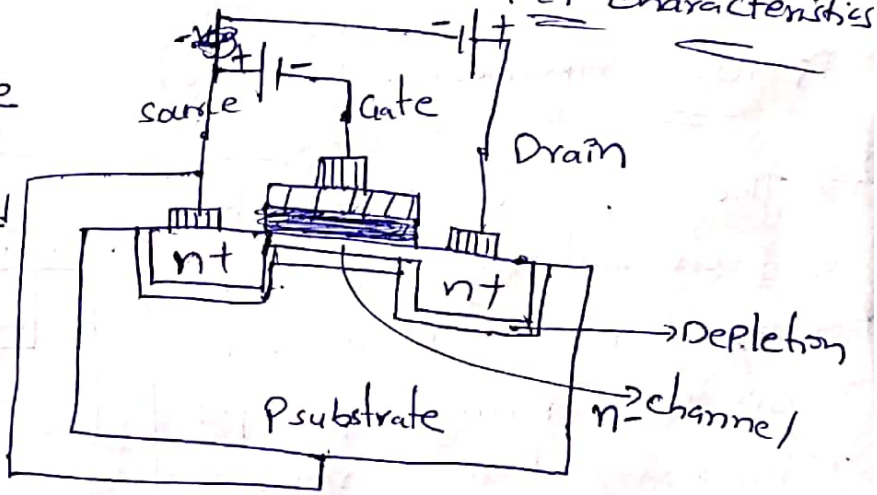
output characteristics



Transfer characteristics

VVImp

NMOS in Depletion mode



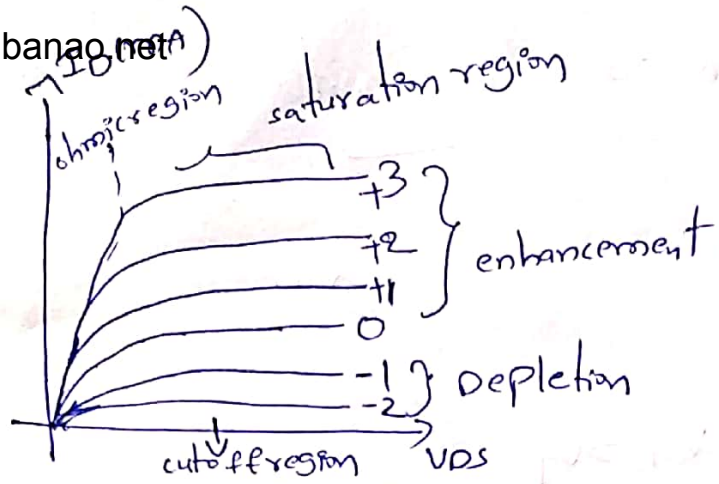
→ The channel is established even at $V_{gs}=0$ by adding suitable impurities between drain & source terminal & before depositing insulation at gate

→ In depletion mode, the source & drain are connected by a conducting channel, the channel width can be controlled by applying suitable negative voltage to the gate terminal.

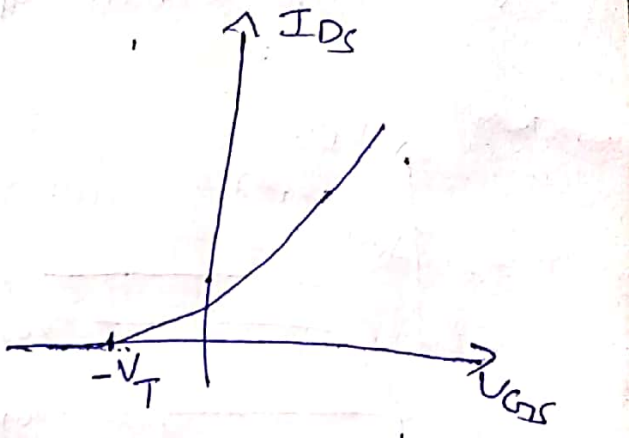
→ If "gate voltage" is negative then as negative V_{gs} increases the current decreases & if the V_{gs} is positive then I_{DS} increases.

→ The depletion MOSFET operates in both modes i.e., in enhancement & depletion modes.

[If V_{GS} = -ve, I_{DS} ↓
V_{GS} = +ve, I_{DS} ↑]



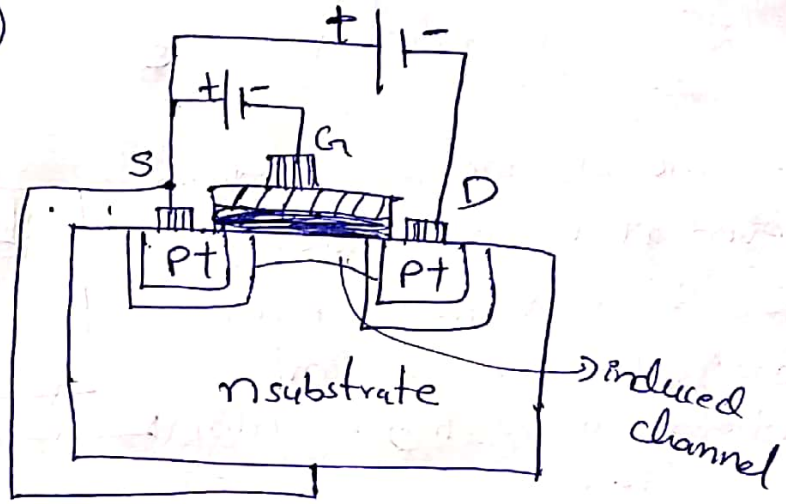
output characteristics
(V_{DS} Vs I_D as V_{GS} constant)



Transfer characteristics

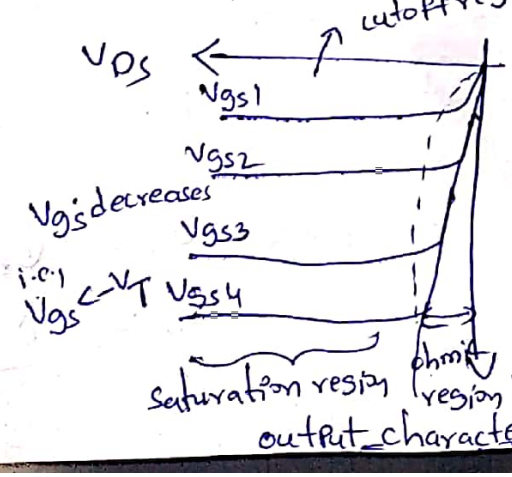
PMOS (enhancement mode)

→ The P-channel MOSFET has a P-channel region between source & drain. The drain & source are heavily doped P+ regions & substrate is n type.

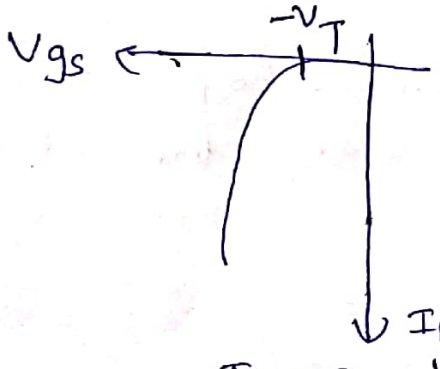


→ The current flow due to the holes. when we apply the negative gate voltage the electrons present under the oxide layer pushed downward into the substrate with a repulsive force. The negative voltage attracts holes from the P+ source & drain regions into the channel.

→ Now, if a voltage is applied between the D & S current flows between the S & D.

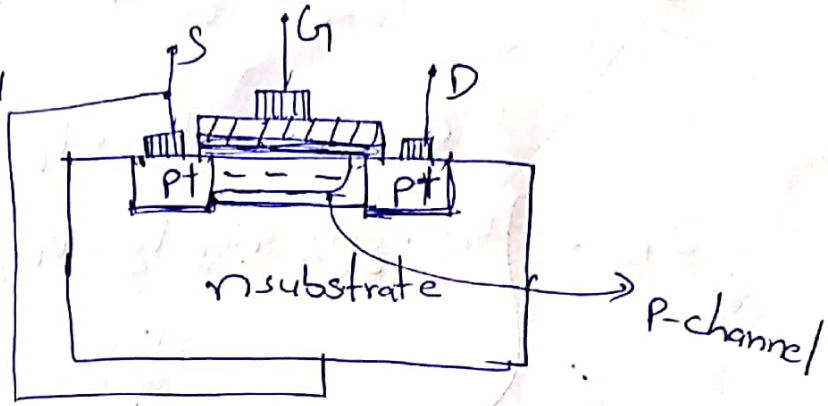


output characteristics



Transfer Characteristics

n Depletion mode :-



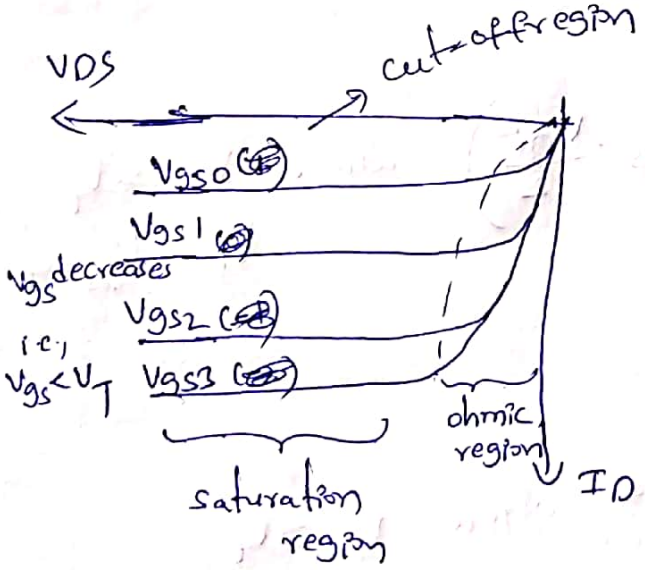
→ The channel is established even at $V_{GS}=0$ by adding suitable impurities between D & S terminal & before depositing ~~insulation~~ insulation at gate.

→ In depletion mode, the S & D are connected by a conducting channel.

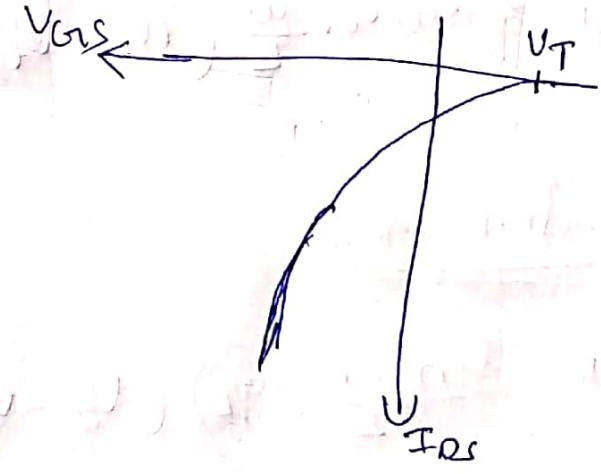
→ If V_{GS} = -ve the I_{DS} increases

V_{GS} = +ve the I_{DS} decreases.

→ The depletion MOSFET operates in both modes i.e., in enhancement & depletion modes.



output characteristics
(V_{DS} Vs I_D where V_{GS} = constant)



Transfer characteristics
(V_{GS} Vs I_D)

current in 3 regions.

cutoff region:-

$I_{DS} = 0$, $V_{gs} < V_t$

linear / triode region:-

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{gs} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right)$$ where $V_{gs} > V_t$, $V_{DS} < V_{gs} - V_t$.

saturation region:-

$$I_D = \frac{\mu_n C_{ox}}{2} (W/L) (V_{gs} - V_t)^2$$ where $V_{gs} > V_t$, $V_{DS} \geq V_{gs} - V_t$.

FET amplifiers:-

The small signal models for the common source FET can be used for analyzing the 3 basic FET amplifier configurations.

1) Common Source (CS)
2) Common Drain (CD) (or) Source-follower.
3) Common Gate (CG).

→ The CS amplifier which provides good voltage amplification is most frequently used.

→ The CD amplifier with high input impedance and near-unity voltage gain is used as a buffer amplifier.

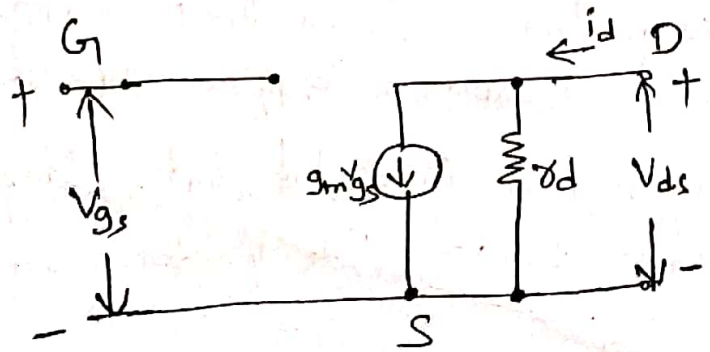
→ The CG amplifier is used as a high-frequency amplifier.

The small signal current source model for the FET in CS configuration.

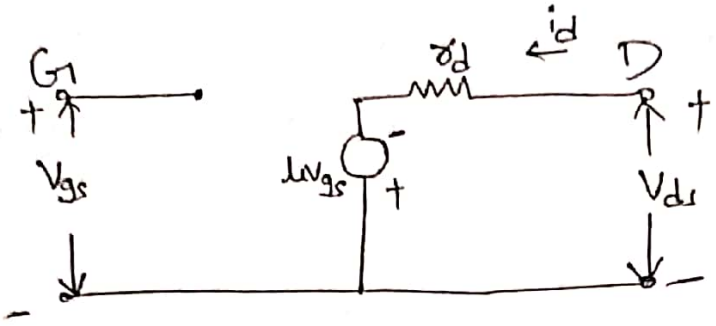
$$i_d = f(V_{gs}, V_{ds})$$

Drain current is a function of V_{gs} and V_{ds}.

$$i_d = g_m V_{gs} + \frac{V_{ds}}{r_d}$$



Small signal voltage source model for FET is CS configuration.



Convert I source to Voltage source

$V = IR$

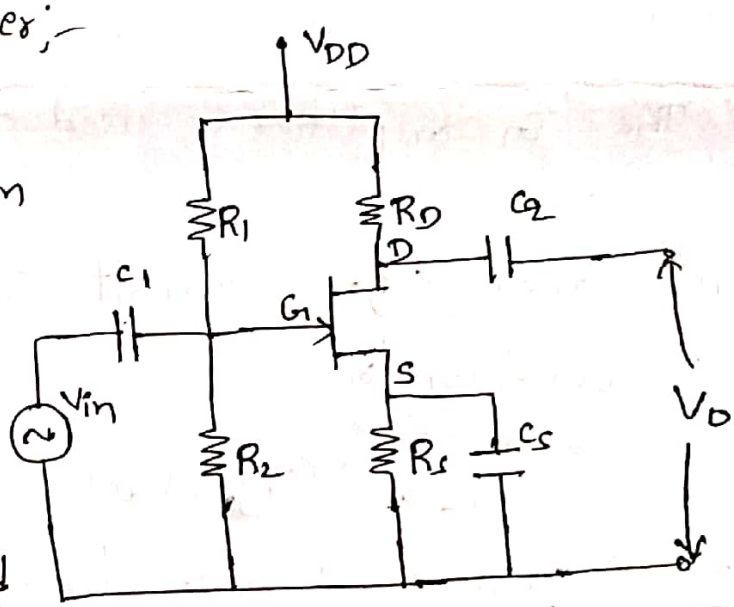
$= g_m V_{gs} r_d$

$V = \mu V_{gs}$

$(\because \mu = g_m r_d)$

Biasing Techniques:- ① Fixed bias
② Voltage divider bias
③ self bias.

Common Source amplifier:-



common source N-channel JFET (Voltage divider bias) amplifie

→ The figure shows common source amplifier in "voltage divider bias" configuration.

→ Here resistors R_1 & R_2 are used to bias the field effect transistor.

→ The capacitors C_1 & C_2 are used to couple the a.c input voltage source & the output voltage respectively.

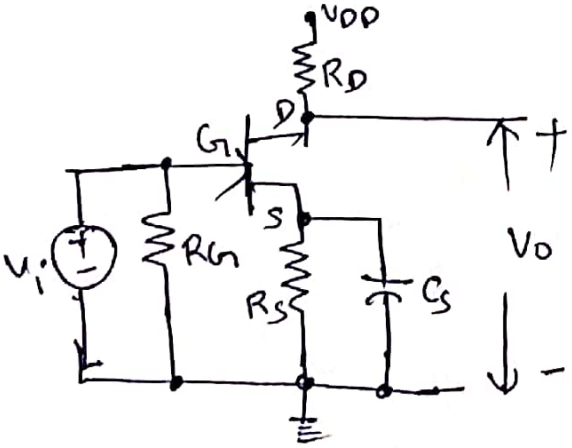
→ The capacitor "C_S" keeps the source of the FET effectively at ac. ground & is known as source bypass capacitor.

Operation: when the a.c signal is fed to gate, it produces Variation is gate to source voltage this produces variation is the drain current.

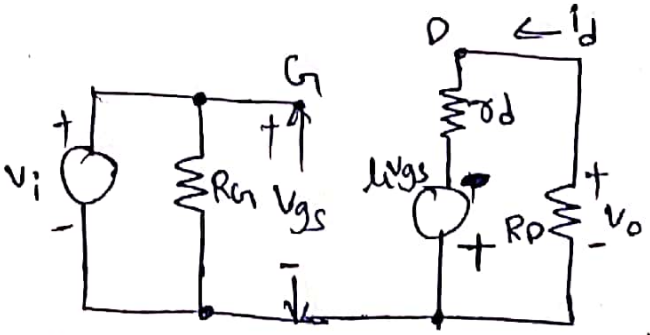
→ As the gate to source voltage (V_{GS}) increases, the drain current also increases. Because of this the voltage drop across the resistor R_D also increases. This causes the drain voltage to decrease. So, there is a phase inversion between output and input.

frequency response of CS amplifier.

→ A simple common-source amplifier & the associated small-signal equivalent circuit using the voltage-source model of FET is shown in figure below.



(a) common source amplifier (self bias)



(b) small signal equivalent circuit of CS amplifier

→ Voltage gain (Av) :- Av is ratio of V_o to V_i

$$V_o = -\mu V_{gs} \frac{R_D}{R_D + r_d}$$

V_{gs} is the input voltage (apply voltage division rule)

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d} \quad (\because V_{gs} = V_i)$$

(2) This source resistor (R_S) is used to set the Q-Point but is bypassed by C_S for mid-frequency operation.

Input impedance: from fig (b) the input impedance is given by

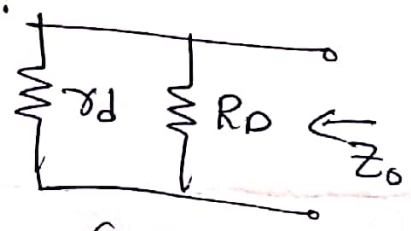
$$Z_i = R_G$$

Output Impedance: output impedance is the impedance measured at the output terminals with the input voltage $V_i = 0$

∴ when $V_i = 0$, $V_{gs} = 0$ & hence $\mu V_{gs} = 0$

Then the equivalent circuit for calculating output impedance is shown in "fig c"

∴ output impedance $Z_o = r_d \| R_D$



(c)

Normally, r_d will be far greater than R_D

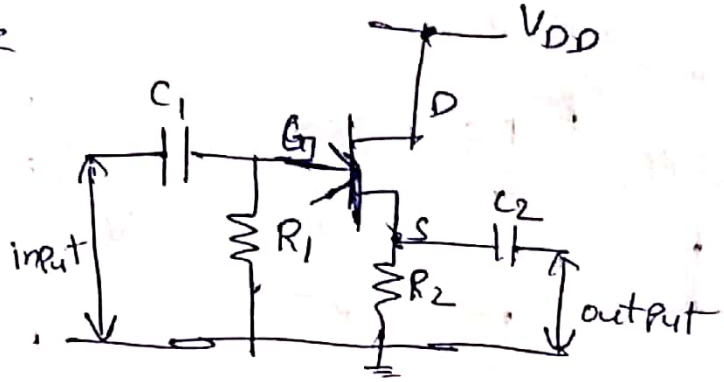
Hence, $\boxed{Z_o \approx R_D}$

(3) Amplifier / source follower:-

This configuration, which is sometimes known as a "source follower", is characterized by a voltage gain of less than unity & features a large current gain as a result of having a very large input impedance & a small output impedance.

→ The typical implementation of the common drain (or) source follower (or) buffer circuit is very easy to realise in a practical fashion.

→ In this Gate (G) is the input terminal & ~~Drain (D)~~ Source (S) is the output terminal



CD amplifier (self bias)

→ The capacitors C_1 & C_2 are used to couple the AC signal between stages & block the DC elements.

→ The resistor "R_1" provides the gate bias, holding the gate at ground potential.

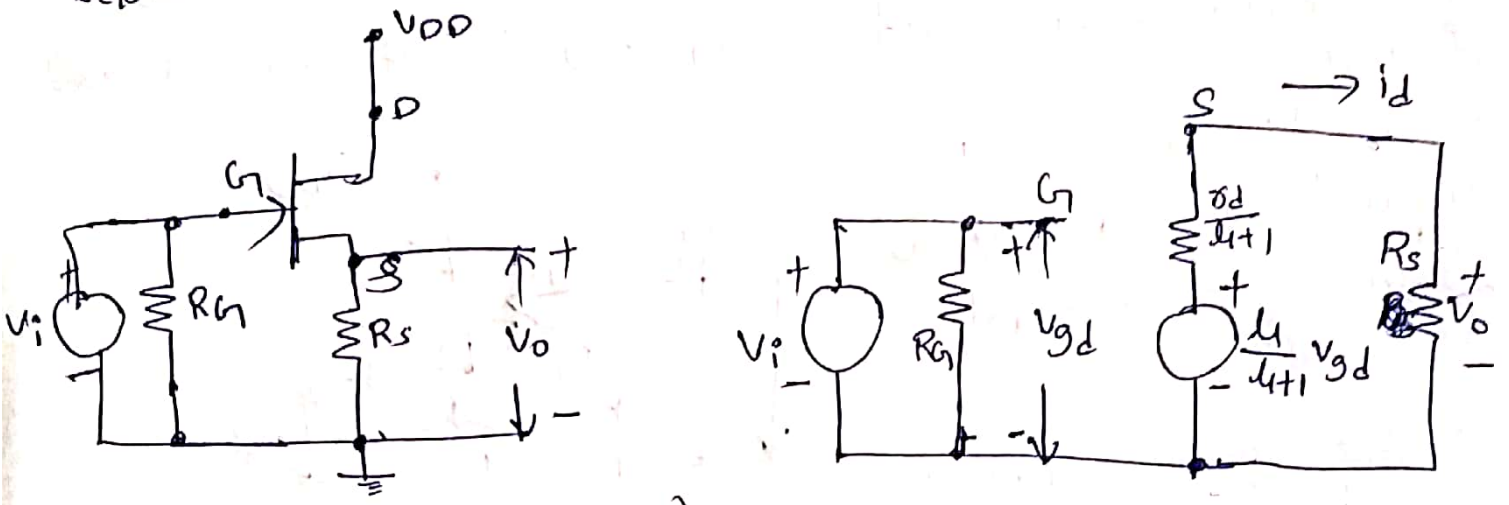
→ The source circuit shows the resistor "R_2" to ground - its value is determined by the channel current that is required.

→ The source follower circuit presents a very high impedance to the preceding stage & it is for this reason that the source follower is an ideal format for use as a buffer.

Common Drain (CD) amplifier / Source follower / Unity voltage amplifier

→ CD amplifier is sometimes known as a source follower is characterized by $A_V \leq 1$.

A simple CD amplifier & the associated small-signal equivalent circuit using the voltage-source model of FET is shown in figure below.



(a) CD amplifier (self bias) (b) Small signal equivalent circuit of a CD amplifier

Voltage gain:- Since V_{gd} is more easily determined than V_{gs}, the voltage source in the output ~~circuit~~ circuit is expressed interms of V_{gd} using Thevenin's theorem. The output voltage V_o is

$$V_o = \frac{\mu}{\mu+1} V_{gd} \frac{R_S}{R_S + \frac{r_d}{\mu+1}} = \frac{\mu R_S V_{gd}}{R_S(\mu+1)+r_d}$$

where $V_{gd} = V_i$, the input voltage

$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{(\mu+1)R_S + r_d}$$

Input impedance:- From figure(b), input impedance $Z_i = R_G$

output impedance:- Z_o measured at the output terminals with $V_i = 0$ can be simply calculated from ⊖ fig(c)

As $V_i = 0$, $V_{gd} = 0$; $\mu/(\mu+1) V_{gd} = 0$

$\therefore Z_o = \frac{r_d}{\mu+1} \| R_S$ when $\mu \gg 1$ $Z_o = \frac{r_d}{\mu} \| R_S = \frac{1}{g_m} \| R_S$ ($\because \mu = g_m r_d$)

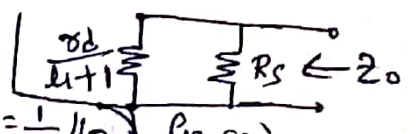


fig (c)