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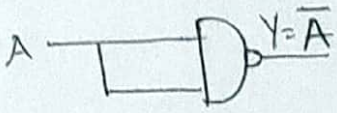
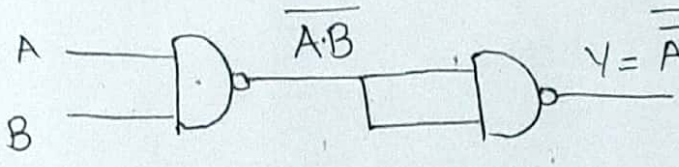
UNIT - IV

(1) (a) Realization of all gates by NAND Gate
(b) Realization of all gates by NOR Gate

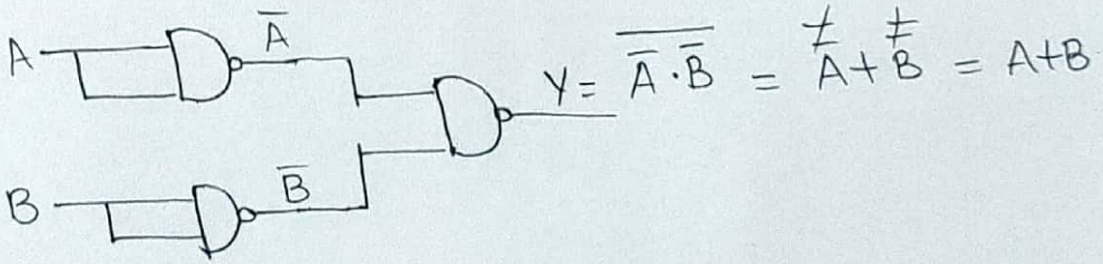
Ans:- (a) (i) NOT Gate



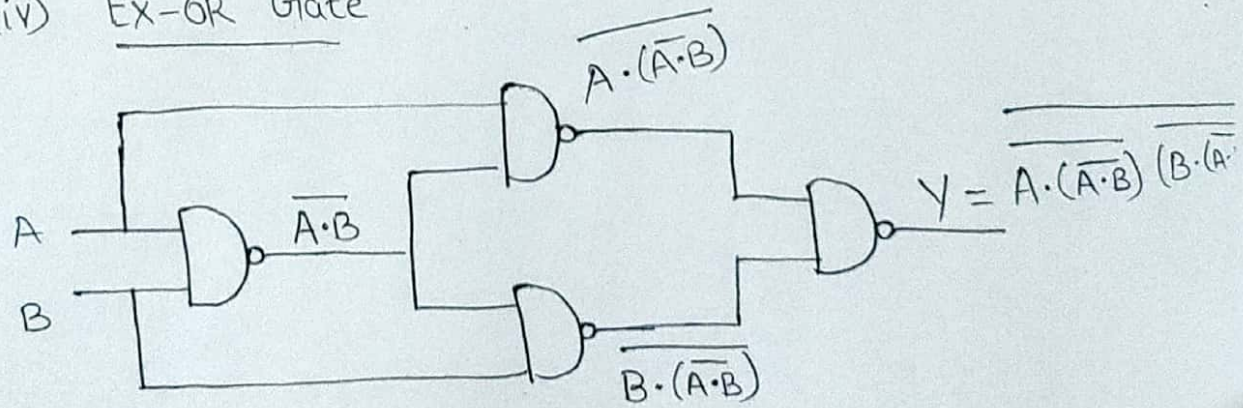
(ii) AND Gate



(iii) OR Gate



(iv) Ex-OR Gate



$$Y = \overline{A\cdot(\overline{A\cdot B})}\ \overline{B\cdot(\overline{A\cdot B})}$$

$$= \overline{\overline{A\cdot(\overline{A\cdot B})}} + \overline{\overline{B\cdot(\overline{A\cdot B})}}$$

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(Q)

$$Y = A\cdot(\overline{A\cdot B}) + B(\overline{A\cdot B})$$

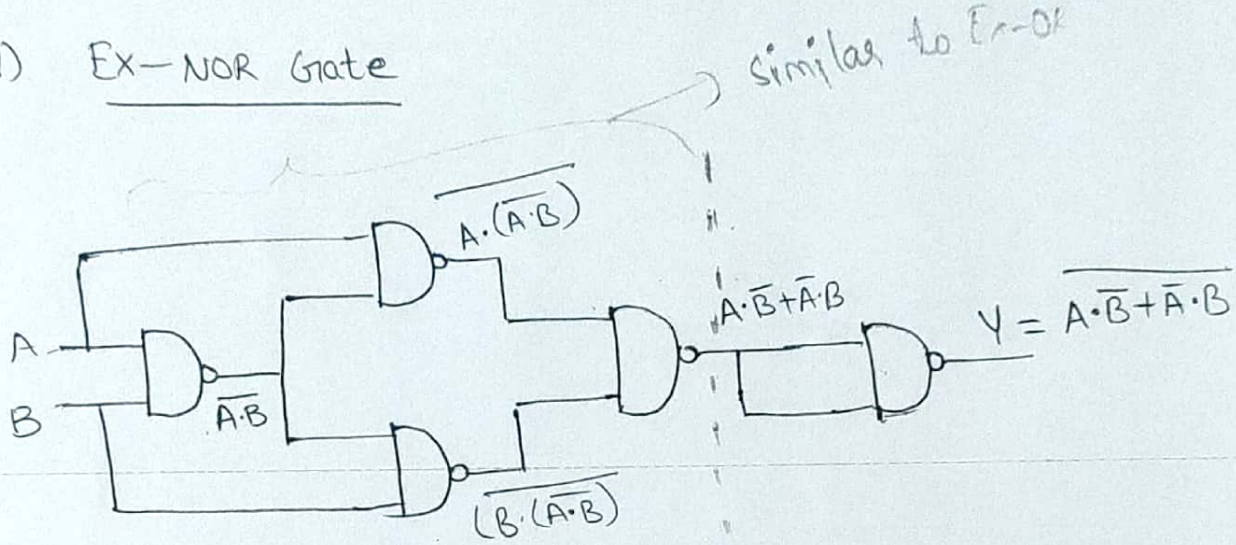
$$= A\cdot(\bar{A}+\bar{B}) + B(\bar{A}+\bar{B})$$

$$= A\cdot\bar{A} + A\cdot\bar{B} + \bar{A}B + B\cdot\bar{B} \qquad (\because A\cdot\bar{A}=0)$$

$$= 0 + A\bar{B} + \bar{A}B + 0$$

$$Y = A\cdot\bar{B} + \bar{A}B = A \oplus B$$

(v) Ex-NOR Gate



$$Y = \overline{A\cdot\bar{B} + \bar{A}\cdot B}$$

$$= (\overline{A\cdot\bar{B}})\,(\overline{\bar{A}\cdot B})$$

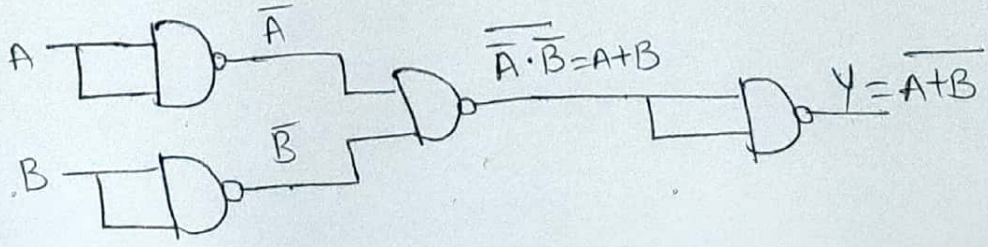
$$= (\bar{A}+\bar{\bar{B}})\,(\bar{\bar{A}}+\bar{B}) = (\bar{A}+B)(A+\bar{B})$$

$$= \bar{A}\cdot A + \bar{A}\bar{B} + AB + B\cdot\bar{B})$$

$$= 0 + \bar{A}\bar{B} + AB + B\cdot\bar{B})$$

$$Y = \bar{A}\bar{B} + AB = \overline{A \oplus B}$$

(vi) NOR Gate



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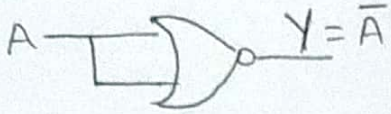
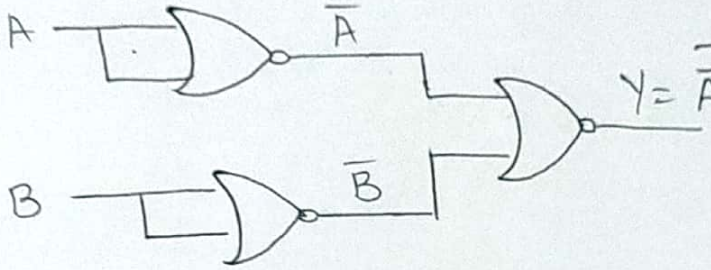
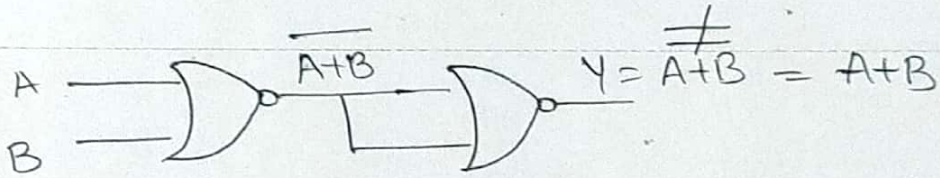
(b) (i) NOT Gate



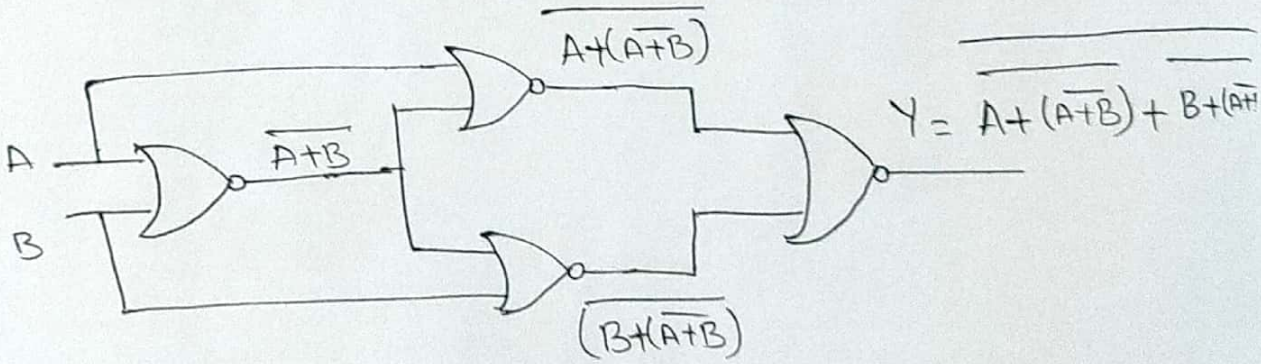
(ii) AND Gate



(iii) OR Gate



(iv) Ex-NOR Gate



$$Y = \overline{A + (\overline{A+B})} + \overline{B + (\overline{A+B})}$$

$$Y = \left(\overline{A + (\overline{A+B})}\right) \cdot \left(\overline{B + (\overline{A+B})}\right)$$

$$= \left(A + (\overline{A+B})\right) \cdot \left(B + (\overline{A+B})\right)$$

$$= \left(A + (\bar{A} \cdot \bar{B})\right) \cdot \left(B + \bar{A} \cdot \bar{B}\right)$$

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$= (A+\bar{A})(A+\bar{B}) \cdot (B+\bar{A}) \cdot (B+\bar{B})$ $\because (A+\bar{A}=1)$

$= 1\,(A+\bar{B}) \cdot (B+\bar{A}) \cdot 1$

$= (A+\bar{B})(B+\bar{A})$

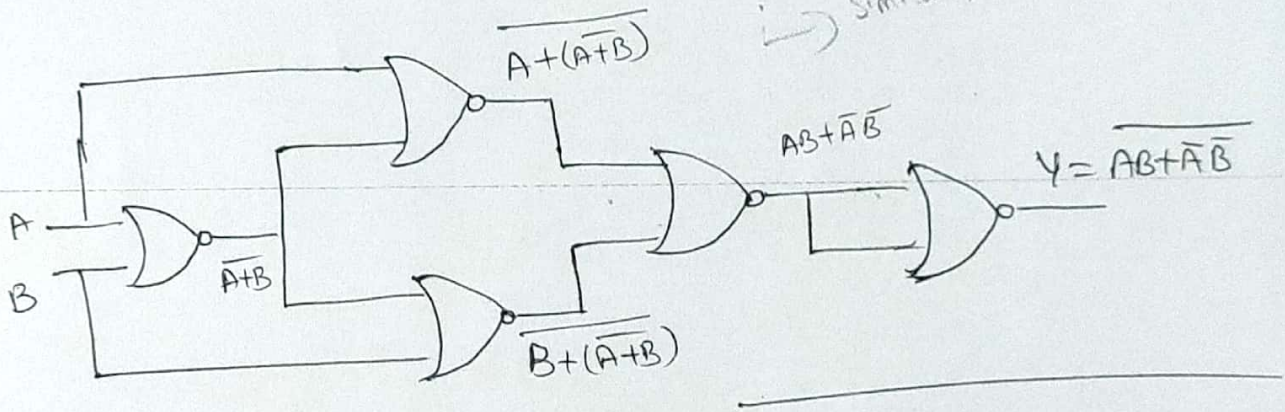
$= AB + A\bar{A} + B\bar{B} + \bar{A}\bar{B}$

$= AB + 0 + 0 + \bar{A}\bar{B}$

$Y = AB + \bar{A}\bar{B} = \overline{A \oplus B}$

(v) EX-NOR Gate:

→ Similar to Ex-NOR



$Y = \overline{AB + \bar{A}\bar{B}}$

$= (\overline{AB})(\overline{\bar{A}\bar{B}})$

$= (\bar{A}+\bar{B})(\bar{\bar{A}}+\bar{\bar{B}})$

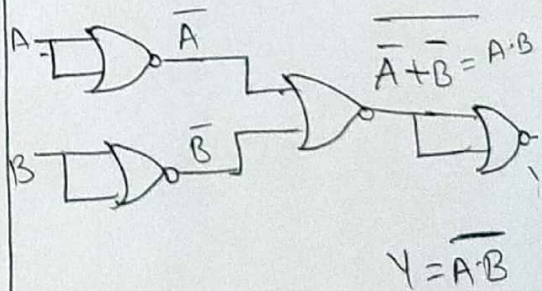
$= (\bar{A}+\bar{B})(A+B)$

$= \bar{A} \cdot A + \bar{A}B + A\bar{B} + B \cdot \bar{B}$

$= 0 + \bar{A}B + A\bar{B} + 0$

$Y = \bar{A}B + A\bar{B} = A \oplus B$

(vi) NAND Gate:



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(2) Explain and design the logic diagram of a circuit for 4 bit parallel Adder / Subtractor?

Ans:-

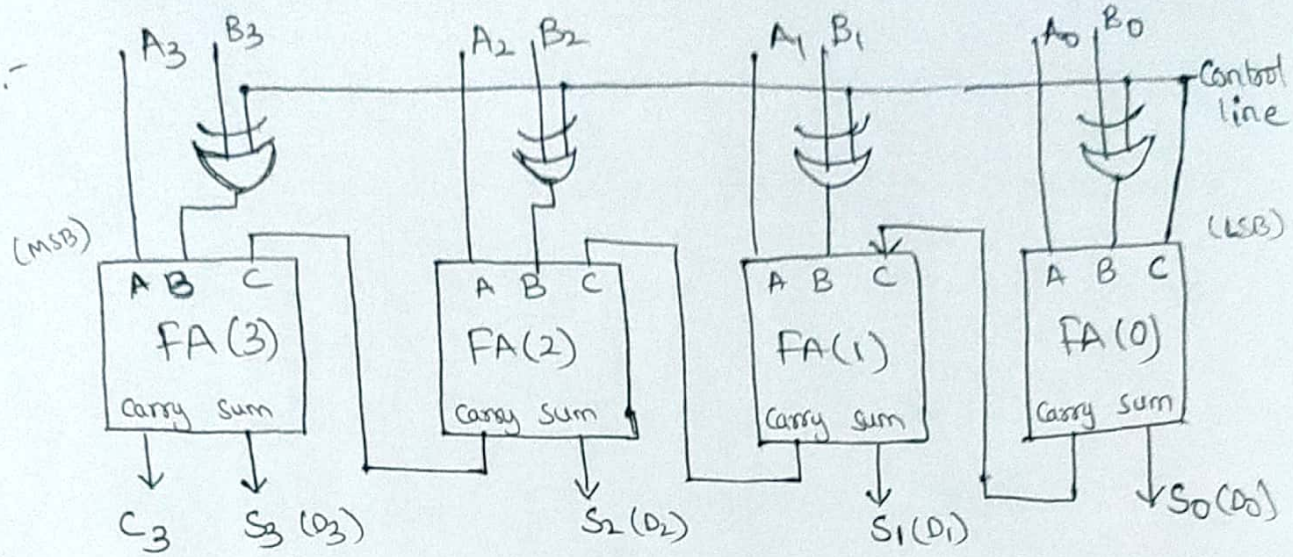

fig: 4 bit parallel adder / Subtractor

→ The 4 bit parallel binary adder / Subractor circuit is shown in above figure.

→ To perform the operation of both 4bit addition and Subtraction. It required 4 full adder's (FA). Each full adder has three inputs (ie., A, B & C) and two outputs (ie., Sum and Carry).

→ for 4 bit parallel adder / Subtractor, it has two 4 bit inputs A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0. The control line, connected with C of the least significant bit (LSB) of the full adder, is used to perform the operations of addition and subtraction.

→ The Ex-OR gates are used as controlled inverters.

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→ In a computer, one has to carry out the addition as well as subtraction. Hence it is more convenient to have a single circuit out both these arithmetic functions instead of two different circuits.

→ The binary subtraction can be converted in to the addition by considering the 2's complement method.

→ In the circuit, when control line = 0, the circuit acts as an adder, the number $B_3\ B_2\ B_1\ B_0$ is added to $A_3\ A_2\ A_1\ A_0$ and gives Sum = $S_3\ S_2\ S_1\ S_0$.

When control line = 1, the circuit acts as subtractor, the number $B_3\ B_2\ B_1\ B_0$ is subtracted from $A_3 A_2 A_1 A_0$ and gives the difference = $D_3\ D_2\ D_1\ D_0$

Operation:

(1) Adder :- When control line = 0, the output of the Ex-OR gates will be same as the B data bits. The carry input to the first full adder is 0 (ie., Control line = 0). Hence A and B bits are applied as the two inputs to the parallel adder. Thus the output would correspond to the sum of A & B.

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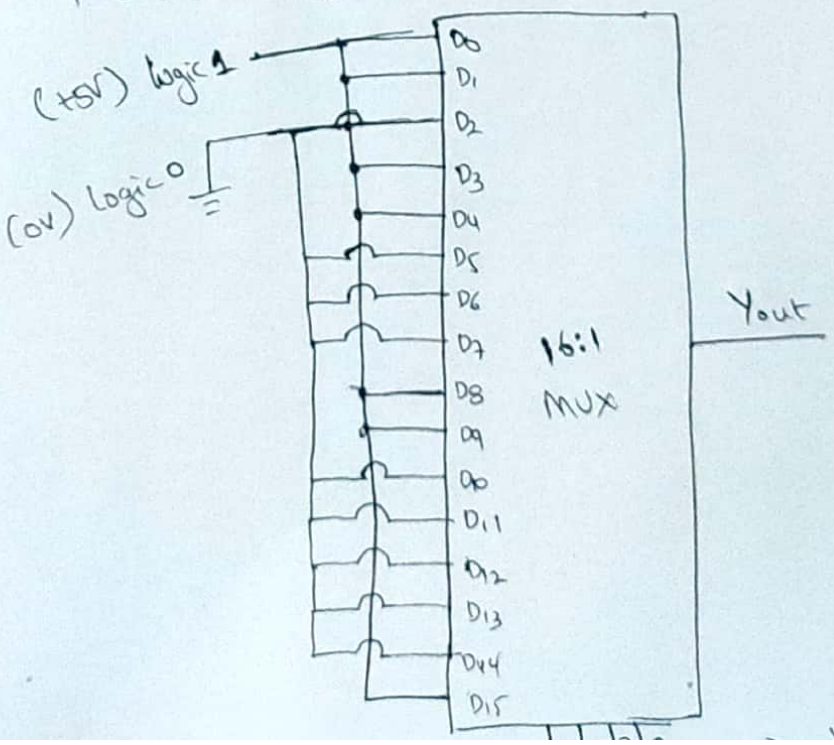
(2) Subtractor: when control line = 1, then the output of the Ex-OR gates will be the complement of the ~~B0 data0 data0~~ B data bits. The carry input to the first full adder is now 1 (i.e., Control line = 1). Hence addition of 1 to the 1's Complement of B bits forms the 2's Complement B bits are applied as the inputs to the parallel adder. This is the process of Subtracting a binary number from another using 2's Complement method.

(3) Implement the logic function $f(A,B,C,D) = \Sigma(0,1,3,4,8,9)$ using (i) 16:1 MUX (ii) 8:1 MUX (iii) 4:1 MUX

Sol (i) 16:1 MUX

$16 = 2^4$

for 16:1 MUX, it has 16 inputs, one output & 4 Select lines.



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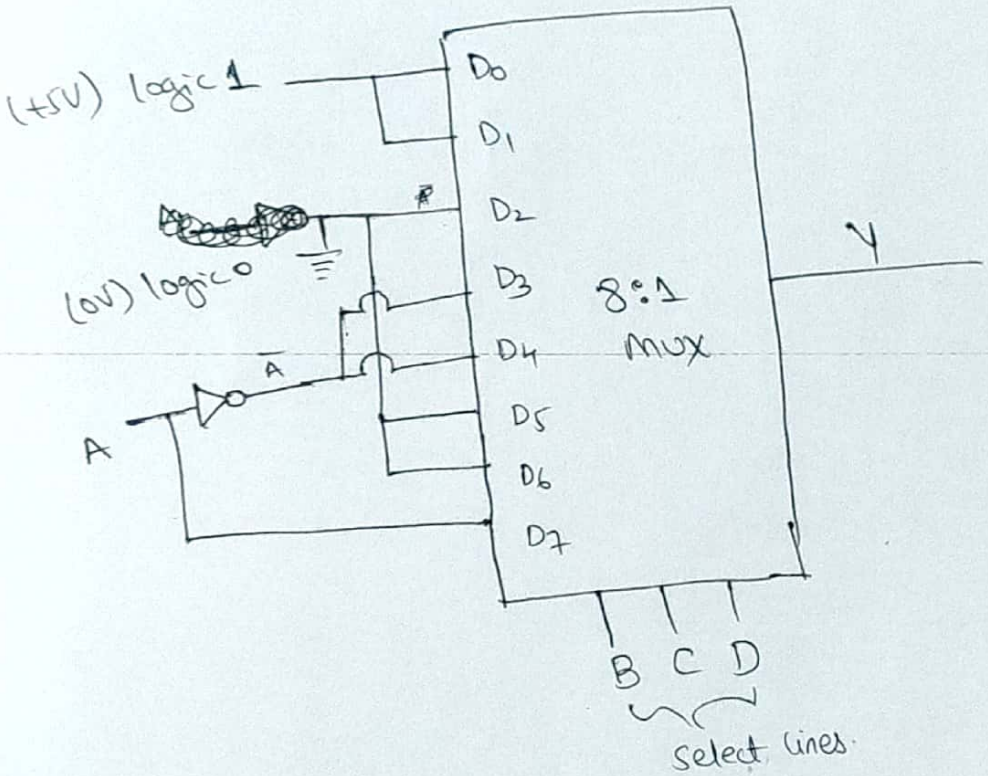
(ii) 8:1 MUX

BCD → inputs are used for selection lines ie.

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A



(iii) 4:1 MUX

CD → inputs are used for select lines.

	D_0	D_1	D_2	D_3
$\bar{A}\bar{B}$	(0)	(1)	2	(3)
$A\bar{B}$	(4)	5	6	7
$\bar{A}B$	(8)	(9)	10	11
AB	12	13	14	(15)
	f_1	f_2	$f_3=0$	f_4

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$$F_1 = \overline{\overline{A}\,\overline{B} + A\overline{B} + \overline{A}B}$$

$$= \overline{A}(\overline{B}+B) + A\overline{B}$$

$$= \overline{A} + A\overline{B}$$

$$= (\overline{A}+A)(\overline{A}+\overline{B})$$

$$\Rightarrow \boxed{f_1 = \overline{A} + \overline{B}} \equiv D_0$$

$$f_2 = \overline{A}\,\overline{B} + \overline{A}B$$

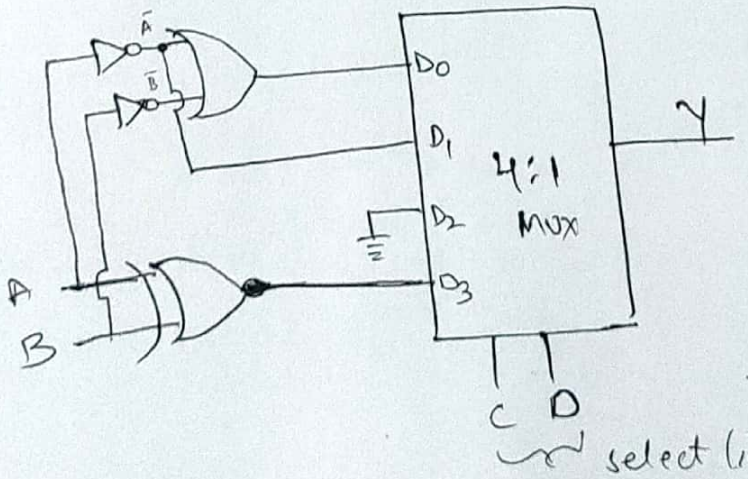
$$= \overline{A}(\overline{B}+B)$$

$$\Rightarrow \boxed{f_2 = \overline{A}} \equiv D_1$$

$$\Rightarrow \boxed{f_3 = 0} \equiv D_2$$

$$f_4 = \overline{A}\,\overline{B} + AB$$

$$\Rightarrow \boxed{f_4 = A \odot B} \equiv D_3$$



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(10)

4) Explain the working of 2 bit comparator?

Ans:- **Comparator:-**

A comparator is a logic circuit that compares the value of two numbers. Let us assume that the bits A & B are compared. The truth table for the comparator action as shown below.

Inputs		Outputs		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Truth table for one bit comparator.

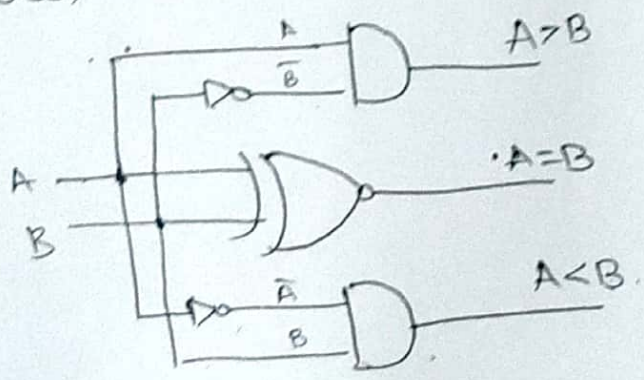
From the truth table, the expression for the outputs A>B, A=B and A<B can be written as

$$A>B \Rightarrow A\cdot\bar{B}$$

$$A=B \Rightarrow \overline{A \oplus B}$$

$$A<B \Rightarrow \bar{A}\cdot B$$

The single bit comparator can be realized by using logic gates,



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Two bit Comparator :—

Let the numbers to be compared be A (A_1 A_0) and B (B_1 B_0).

→ A will be greater than B when any one of the following conditions is satisfied.

① when $A_1 = 1$, $B_1 = 0$ irrespective of other bits

② If $A_1 = B_1$ and $A_0 = 1$, $B_0 = 0$.

→ A will be Equal to B when the following conditions satisfied.

① $A_1 = B_1$, $A_0 = B_0$.

→ A will be less than B when any one of the following conditions is satisfied.

① when $A_1 = 0$, $B_1 = 1$ irrespective of other bits

② If $A_1 = B_1$ and $A_0 = 0$, $B_0 = 1$

→ To represent these conditions in the form of a truth table, it requires 16 combinations & hence a function table is given as.

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Inputs		outputs		
A_1 & B_1	A_0 & B_0	$A>B$	$A=B$	$A<B$
$A_1 > B_1$	X	1	0	0
$A_1 < B_1$	X	0	0	1
$A_1 = B_1$	$A_0 > B_0$	1	0	0
$A_1 = B_1$	$A_0 < B_0$	0	0	1
$A_1 = B_1$	$A_0 = B_0$	0	1	0

Function table of 2 bit Comparator.

→ In the function table, a X indicates the dont care condition. From the function table, the expressions for $A>B$, $A=B$ & $A<B$.

$$A>B \Rightarrow A_1\overline{B_1} + \overline{A_1 \oplus B_1} \cdot A_0\overline{B_0}$$

$$A=B \Rightarrow \overline{A_1 \oplus B_1} \cdot \overline{A_0 \oplus B_0}$$

$$A<B \Rightarrow \overline{A_1}B_1 + \overline{A_1 \oplus B_1} \cdot \overline{A_0}B_0.$$

→ The two bit comparator can be realized by using logic gates,

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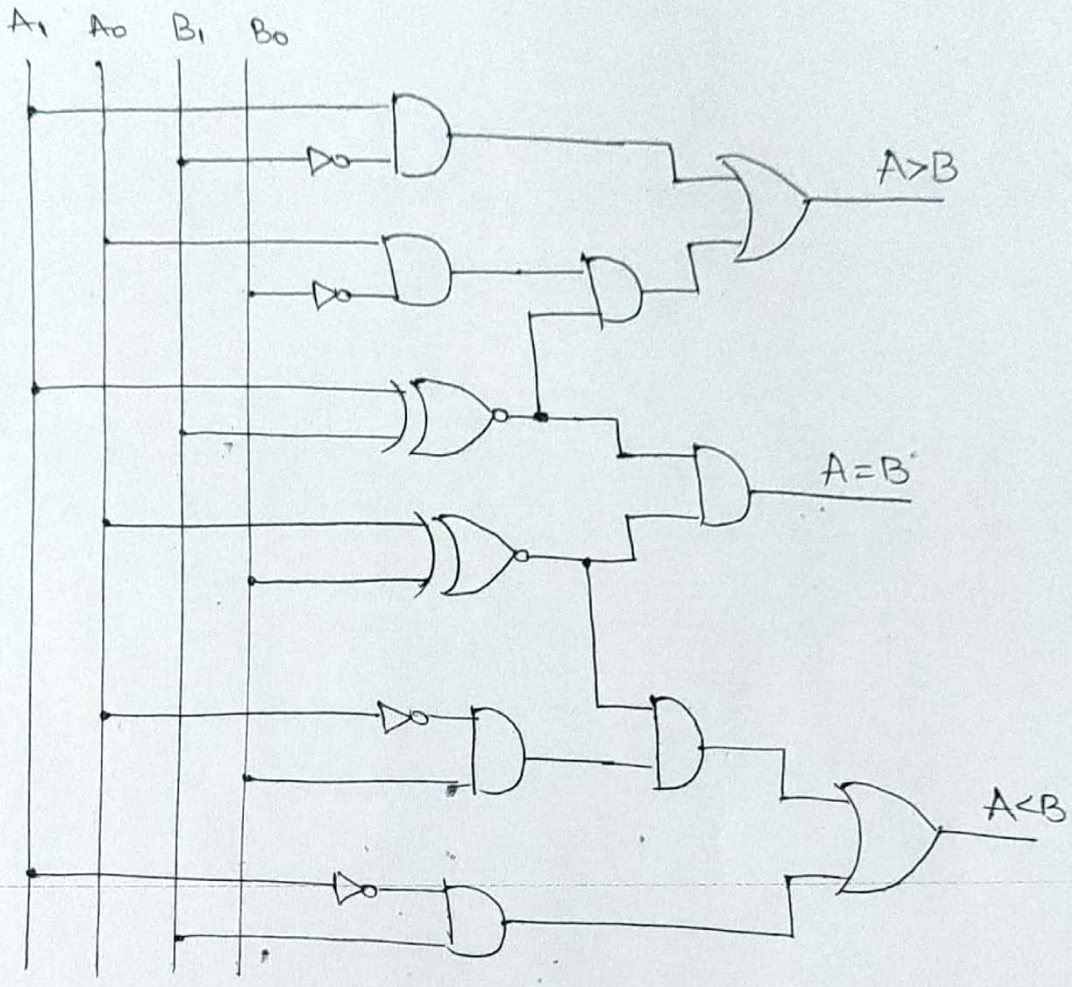

(5) Explain about Encoders and Decoders with Suitable Examples?

Ans:- Encoders:

→ The Encoder Circuit is used to Convert one form of data in to binary form.

→ The input of data may be in form other than binary ie.> decimal, octal, hexadecimal etc.

→ Encoders are required at the interface of man-machine Communication and for transmission of data between the various digital subsystem that do not employ the same code.

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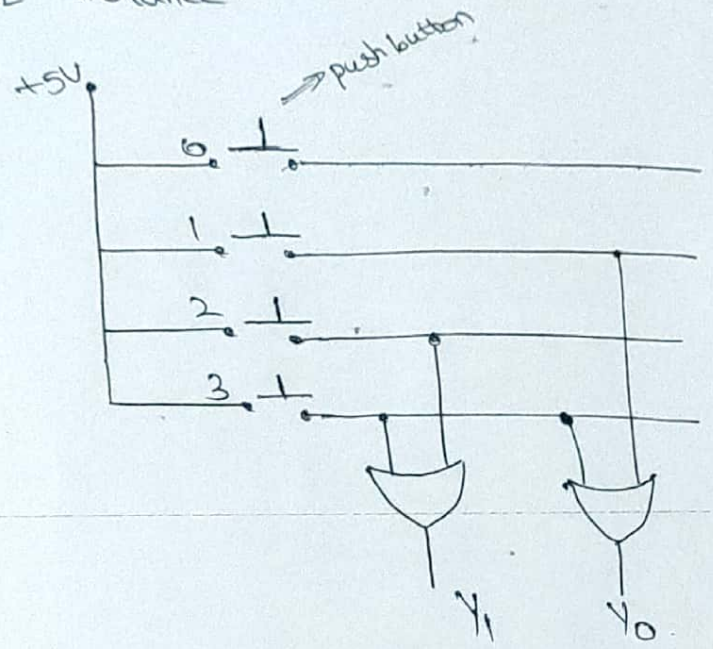
→ The Encoders can also be designed using combinational logic circuits.

→ The circuit diagram of 4×2 Encoder, this circuit converts decimal numbers 0, 1, 2 and 3 in to binary for instance.



4×2 Encoder

Position of the push button (Input)	Outputs	
	Y_1	Y_0
0	0	0
1	0	1
2	1	0
3	1	1

Table of 4×2 Encoder

→ When push button 0 is pressed, the Y_1 and Y_0 OR gates have low outputs, therefore output word is $Y_1 Y_0 = 0$.

→ If the button 1 is keyed, the Y_1 and Y_0 OR gates have low and high outputs, therefore the output word is $Y_1 Y_0 = 01$.

→ Similarly when the button 2 is keyed the output word is $Y_1 Y_0 = 10$

→ When the button 3 is keyed the output word is $Y_1 Y_0 = 11$

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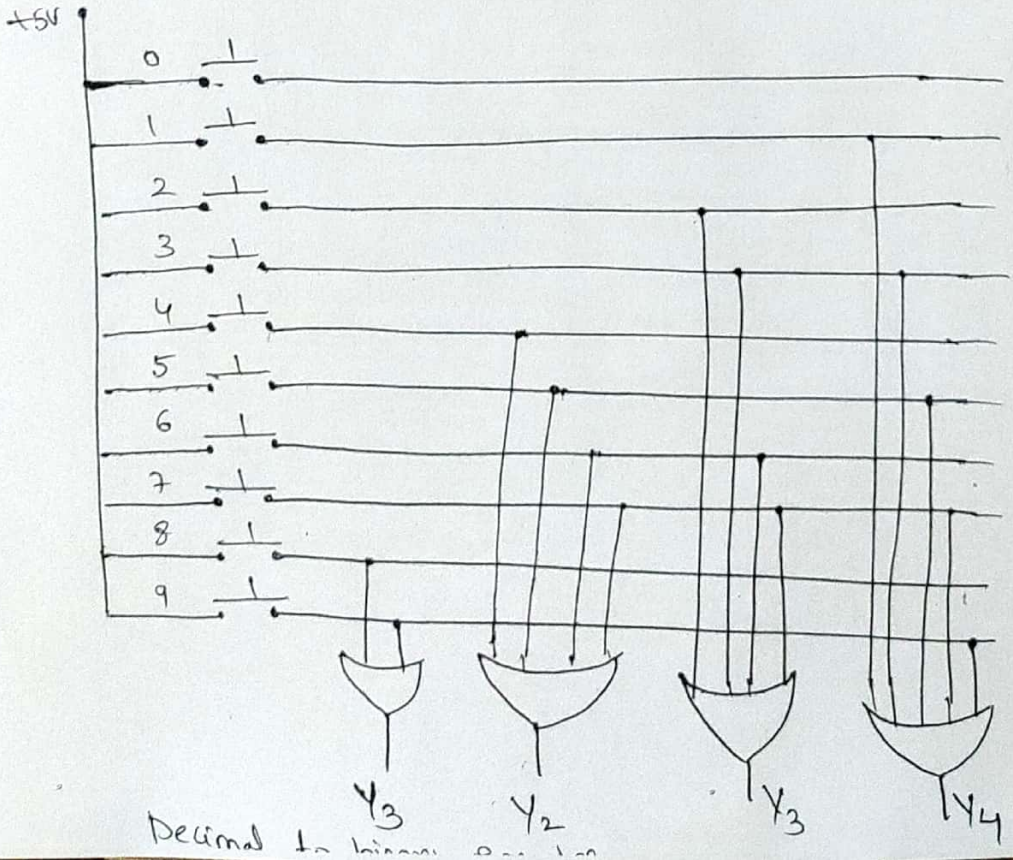
Decimal to binary Encoder:-

position of the push button (input)	outputs			
	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table of Decimal to binary Encoder.



Decimal to binary

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Decoders:

→ The decoder is the opposite of the Encoder.

→ This circuit converts binary data in to other form ie., decimal, octal, hexadecimal etc.

→ Decoder is a combinational logic circuit which accepts the states from various inputs and delivers a logic 1 at any one of the 2^n outputs.

→ Thus the decoder circuits of 2 input lines gives $2^2 = 4$ outputs, similarly the 3 input decoder gives $2^3 = 8$ outputs.

2×4 Decoder: [2 inputs, 4 outputs]

→ When the inputs A & B are 0 then the output of Y_0 AND gate is 1 because all inputs of the Y_0 gate is high & outputs of other AND gates are low, because atleast one input is low for these.

→ for inputs A = 0 & B = 1, then $Y_1 = 1$.
for inputs A = 1 & B = 0, then $Y_2 = 1$
for inputs A = 1 & B = 1, then $Y_3 = 1$

→ Therefore in an decoder only one output is high for one combination and other outputs low.

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Inputs		Outputs			
A	B	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table of 2×4 Decoder

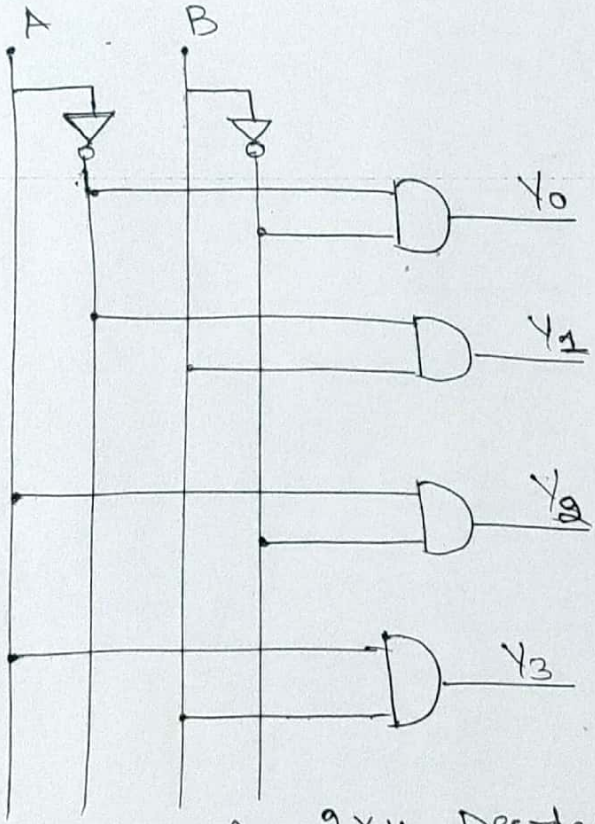

fig: 2×4 Decoder.

3×8 Decoder:

→ For instance when A=0, B=0 & C=0, the Y_0 AND gate has all high inputs, therefore the Y_0 is high. Further more, all other AND gates have atleast one low input as a result all other AND gates have low outputs.

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Inputs			Outputs							
A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Table of 3x8 Decoder.

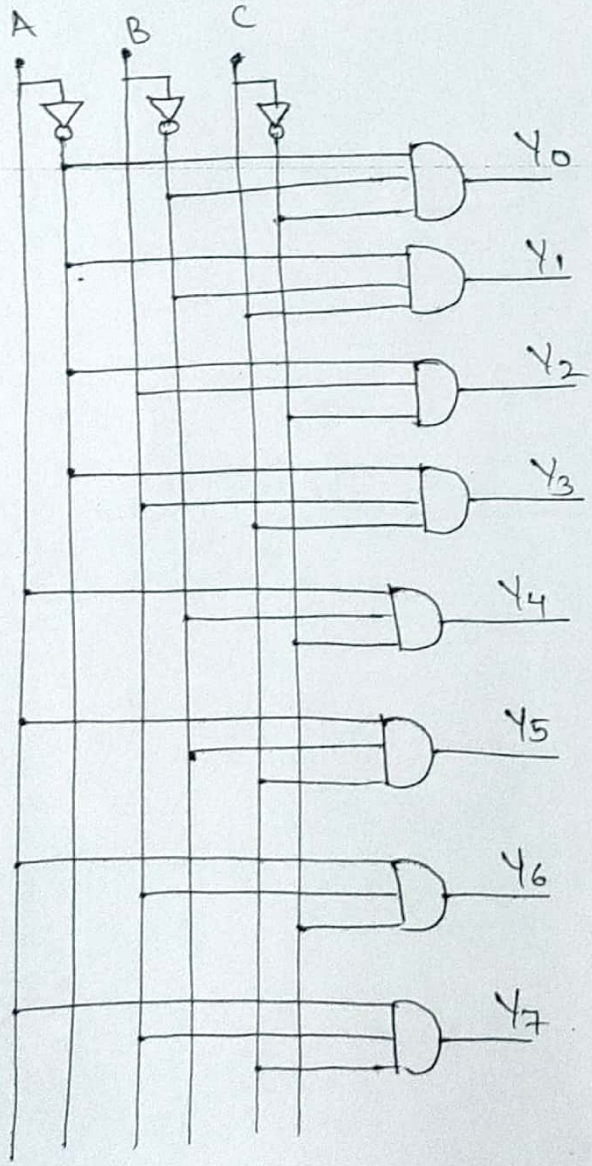

fig: 3x8 decoder.

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(6) (a) Simplify the following function using K-map method

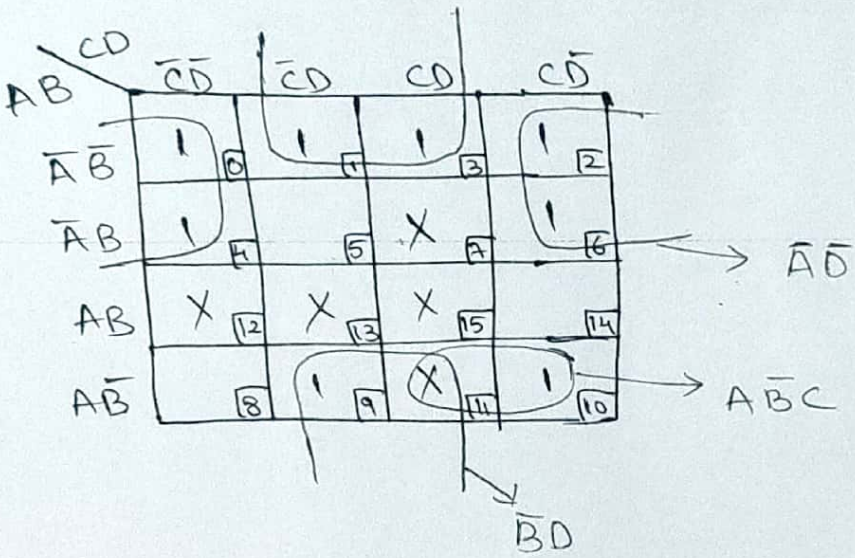
$F(A,B,C,D) = \Sigma(0,1,2,3,4,6,9,10) + d(7,11,12,13,15)$

(b) Simplify the following function using K-map method

obtain (i) minimal SOP & (ii) minimal POS Expression.

$F(w,x,y,z) = \Sigma(0,2,3,6,7) + d(8,10,11,15)$

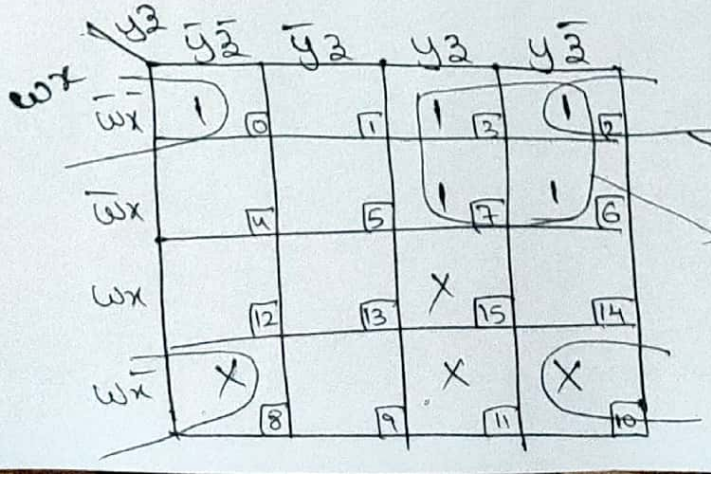
Ans: (a) $F(A,B,C,D) = \Sigma(0,1,2,3,4,6,9,10) + d(7,11,12,13,15)$



$F(A,B,C,D) = \bar{A}\bar{D} + A\bar{B}C + \bar{B}D$.

(b) (i) minimal SOP.

$F(w,x,y,z) = \Sigma(0,2,3,6,7) + d(8,10,11,15)$.



$\therefore F(w,x,y,z) = \bar{x}\bar{z} + \bar{w}y$

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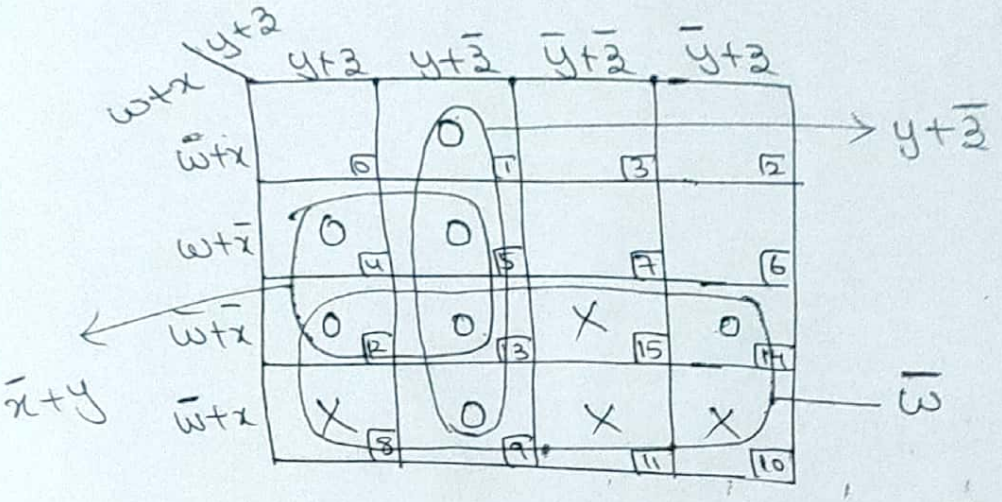
(20)

(ii) Minimal POS Expression:

given $F(w,x,y,z) = \Sigma(0,2,3,6,7) + d(8,10,11,15)$

POS $\overline{F(w,x,y,z)} = \Pi(1,4,5,9,12,13,14) + d(8,10,11,15)$.



minimal POS $F(w,x,y,z) = (\bar{w})(y+\bar{z})(\bar{x}+y)$

Short Answers:-

(1) (a) list the properties of boolean Algebra?

(b) State Duality & Demorgan's theorem?

Ans: (a) properties of Boolean Algebra:-

→ Boolean algebra is a mathematical system consisting of a set of two (or) more distinct elements, "two binary" operators denoted by the symbols (+) & (·) and one "unary" operator denoted by the symbol either bar (-) or prime (').

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① Commutative property:

$$A+B = B+A$$
$$A \cdot B = B \cdot A$$

② Associative property:

$$A+(B+C) = (A+B)+C$$
$$A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

③ Distributive property:

$$A+BC = (A+B)(A+C)$$
$$A \cdot (B+C) = (A \cdot B) + (A \cdot C)$$

④ Complementary property:

$$A+\bar{A} = 1$$
$$A \cdot \bar{A} = 0$$

⑤ Involution property:-

$$(A')' = A \quad (\text{or}) \quad \bar{\bar{A}} = A$$

⑥ Idempotancy property:-

$$A+A = A$$
$$A \cdot A = A$$

⑦ Absorption Law:

$$A+\bar{A}B = A+B.$$

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(8) Consensus law:

$$xy + \bar{x}z + yz = xy + \bar{x}z$$

↳ This law is used to eliminate redundant term from the boolean expression.

(6) Duality Theorem :-

The duality of the function can be obtained by interchanging OR (+) ⟷ AND (·) & AND (·) ⟷ OR (+)

Ex:- (1) $Y = x + y$

Y_d (duality function) $= x \cdot y$.

(2) $F = \bar{A}B + CD$

$F_d = (\bar{A} + B) \cdot (C + D)$

Demorgan's Theorem :-

→ Demorgan's 1st Theorem:

It stated as, the complement of a product of variables is equal to the sum of individual complement of the variables

$$\overline{AB} = \bar{A} + \bar{B}$$

A	B	$\overline{AB}$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

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→ Demorgan's 2nd Theorem :-

It stated as, the complement of a sum of variables is equal to the product of individual complement of the variables

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

A B	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0 0	1	1
0 1	0	0
1 0	0	0
1 1	0	0

(2) (a) Simply the given Expression

$$Y = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$$

(b) Find the Complement of the expression

$$Y = ABC + AB\bar{C} + \bar{A}\bar{B}C + \bar{A}BC$$

Ans: (a) $Y = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$

$= \bar{B}\bar{C}(\bar{A}+A) + A\bar{B}C + AB(C+\bar{C})$

$= \bar{B}\bar{C} \cdot 1 + A\bar{B}C + AB \cdot 1$

$= \bar{B}\bar{C} + A\bar{B}C + AB$

$= \bar{B}(\bar{C} + AC) + AB$

$= \bar{B}((\bar{C}+A)(\bar{C}+C)) + AB$

$= \bar{B}((\bar{C}+A) \cdot 1) + AB$

$= \bar{B}(\bar{C}+A) + AB$

$= \bar{B}\bar{C} + A\bar{B} + AB$

$= \bar{B}\bar{C} + A(B+\bar{B})$

$Y = A + \bar{B}\bar{C}$ //

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(b) $Y = ABC + AB\bar{C} + \bar{A}\bar{B}C + \bar{A}BC$

$$\bar{Y} = \overline{ABC + AB\bar{C} + \bar{A}\bar{B}C + \bar{A}BC}$$

$$= \overline{AB(C+\bar{C}) + \bar{A}C(\bar{B}+B)}$$

$$= \overline{AB \cdot 1 + \bar{A}C \cdot 1}$$

$$= \overline{AB + \bar{A}C}$$

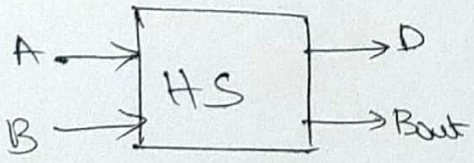
$$= (\overline{AB})\,(\overline{\bar{A}C})$$

$$\bar{Y} = (\bar{A}+\bar{B})\,(A+\bar{C}) \;//$$

(3) What is a half-subtractor? write its truth table?

Ans: The half subtractor is a combinational circuit which is used to perform subtraction of two bits.

→ It has two inputs, A (minuend) and B (subtrahend) and two outputs D (Difference) & Bout (Borrow out).



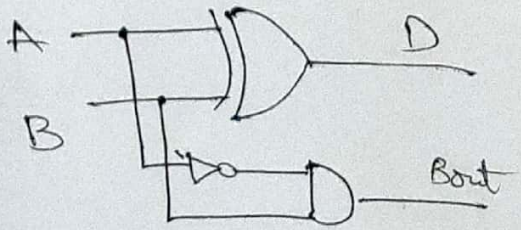
@ Logic Symbol

Inputs		outputs	
A	B	D	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth table

$D = A \oplus B$

$Bout = \bar{A}B$



Logic Diagram

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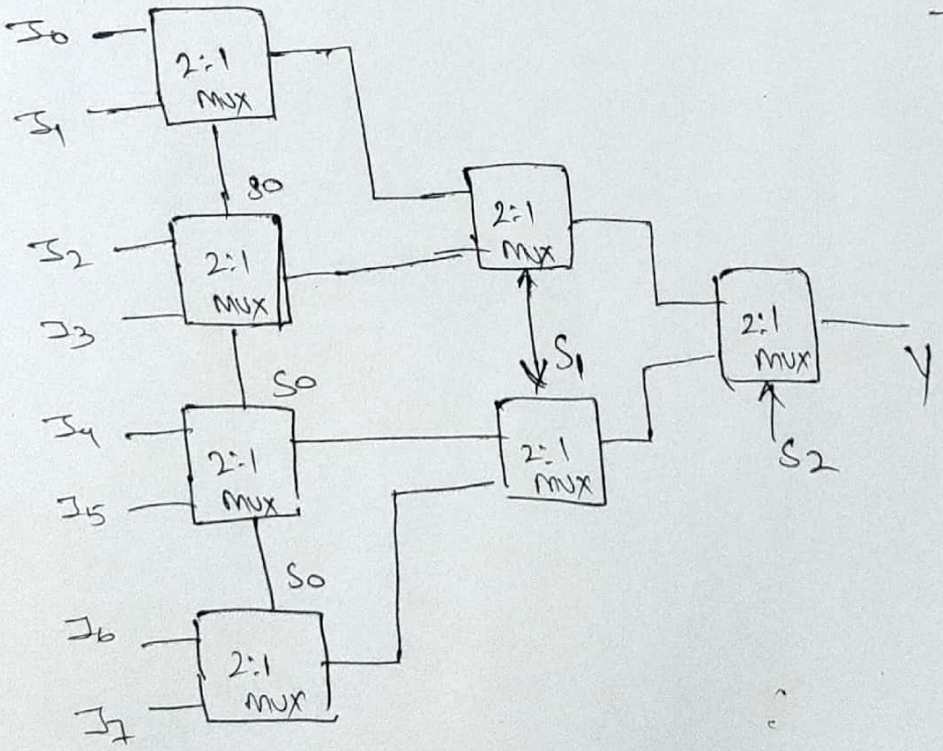
(4) Difference between Serial and parallel Adders?

Ans:-

Serial Adder	parallel Adder
(1) It is slower	(1) It is faster
(2) only one bit can add at a time	(2) All the bits can be added simultaneously
(3) only one full adder is required irrespective of number of bits	(3) Number of full adders required is equal to number of bits
(4) Economical	(4) costly

(5) Design 8:1 mux by using 2:1 mux?



$\frac{8}{2} = 4 \rightarrow 1^{st}$ stage

$\frac{4}{2} = 1 \leftarrow 2^{nd}$ stage

$\frac{2}{2} = 1 \therefore 3^{rd}$ stage

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(6) List the applications of Encoders & decoders.

Ans: Applications:

Encoders: These are used to convert one form of data into binary. These are used as

1. Decimal to Binary Converters (BCD)
2. octal to Binary Converters
3. Hexadecimal to Binary Converters
4. Used to drive 7 segment displays.

Decoders: These are used to convert binary data in to other form. These are used as

1. BCD to decimal Conversion
2. Binary to octal Conversion
3. Hexadecimal to Binary Conversion.
4. BCD to gray (or) gray to BCD conversion.

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