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Code No: 153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, April/May - 2023
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, CSBS, CSIT, CE(SE), CSE(CS), CSE(DS), CSE(N), AI&DS, AI&ML, CSD)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What is a computer?	[2]
b)	Explain functionalities of CPU.	[3]
c)	What are different addressing modes?	[2]
d)	Discuss about any two types of instruction formats.	[3]
e)	Give an example of decimal representation.	[2]
f)	Explain about BCD adder.	[3]
g)	What is magnetic tape?	[2]
h)	Describe parallel priority interrupt.	[3]
i)	What are conditions for incoherence?	[2]
j)	What are CISC characteristics?	[3]

PART – B

(50 Marks)

2.a)	Explain about computer design and architecture.	
b)	What are computer registers? Explain.	[5+5]
	OR	
3.a)	Discuss about shift microoperations in detail.	
b)	List and explain about memory-reference instructions.	[5+5]
4.a)	What are shift instructions? Explain with suitable examples.	
b)	Define control memory. Explain.	[5+5]
	OR	
5.a)	Explain about microinstruction format in detail.	
b)	What are RISC instructions? Explain.	[5+5]
6.a)	Discuss about complements in data representation.	
b)	Explain decimal arithmetic operations with examples.	[5+5]
	OR	
7.a)	Describe fixed-point representation in detail.	
b)	Discuss about division algorithms with examples.	[5+5]

8.a) Explain hardware organization and match logic of associative memory.
b) What are various modes of transfer? Explain. [5+5]

OR

9. Discuss about direct mapping and set associative mapping. [10]

10. Explain the following:
a) Interprocessor arbitration
b) Four-segment instruction pipeline. [5+5]

OR

11. Explain the following:
a) Interprocess communication and synchronization
b) Array processors. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, August/September - 2022

COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to CSE, CSBS, CSIT, CSE(SE), CSE(CS), CSE(AIML), CSE(DS), CSE(N))

Time: 3 Hours **Max.Marks:75**

Answer any five questions

All questions carry equal marks

- - -

1.a)	What is the difference between Computer Organization and Computer Architecture?	
b)	Write a short note on instruction code format.	[8+7]
2.a)	Explain the format of Register reference instructions and their functionalities.	
b)	Draw and explain the flowchart for interrupt cycle.	[8+7]
3.a)	Define the following terms: i) Control memory ii) Address sequencing	
b)	Explain about the microinstruction format with neat sketch.	[8+7]
4.a)	Explain about various addressing modes.	
b)	Briefly explain about General purpose registers and Flag registers.	[7+8]
5.a)	Explain the flow chart for addition operation with sign-magnitude data.	
b)	Perform (-25) + (-10) in binary with negative numbers in 2's complement.	[8+7]
6.a)	Explain the Booth's algorithm for signed multiplication.	
b)	Draw the flowchart for floating point division.	[8+7]
7.a)	Explain the block diagram of I/O interface.	
b)	Write a short note on Cache memory.	[8+7]
8.a)	Explain about instruction pipelining with an example.	
b)	Discuss about the serial arbitration technique.	[8+7]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2021
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Discuss the functional units of a digital computer.
b) Demonstrate construction of a common bus system with multiplexers. [7+8]

2.a) Design a 4-bit combinational circuit decrementer using four full-adder circuits.
b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? [7+8]

3.a) Discuss the need of memory stack and stack limits.
b) Explain the general register organization of the processor. [7+8]

4. Explain addition and subtraction of floating point numbers with an example and necessary flowchart. [15]

5.a) A two way set associative cache has lines of 16 bytes and a total size of 8 K bytes. The 64 Mbytes main memory is byte addressable. Show the format of main memory address.
b) How does SDRAM differ from ordinary DRAM? [8+7]

6.a) Explain the major differences between the central computer and peripheral. How to resolve these differences?
b) Discuss the Strobe control method of Asynchronous data transfer. [8+7]

7.a) What is parallel processing? Explain Flynn's classification of computer.
b) Illustrate vector operations and vector processing. [8+7]

8.a) Discuss about RISC Pipeline.
b) What is cache coherence problem? Discuss solutions for it. [7+8]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2022
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, CSBS, CSIT, CSE(SE), CSE(CS), CSE(AIML), CSE(DS), CSE(N))

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a)	Explain in detail computer design and computer architecture.	
b)	Explain in detail life cycle of instruction.	[9+6]
2.	Explain the following. a) Register transfer. b) Input-Output and interrupt.	[7+8]
3.	Explain in detail various types of addressing modes with examples.	[15]
4.a)	Explain in detail about data transfer instructions.	
b)	Discuss the various types of instruction formats.	[7+8]
5.a)	Explain floating point representation of decimal numbers.	
b)	Explain the decimal addition operation with a neat diagram.	[7+8]
6.a)	Explain the subtraction operation with signed 2's complement data.	
b)	Explain in brief fixed point data representation.	[6+9]
7.a)	Explain the working process of DMA.	
b)	Compare cache and main memory.	[9+6]
8.a)	Explain in brief inter-processor communication.	
b)	Discuss the characteristics of multi-processors.	[8+7]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, October - 2020
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Draw the bus system for four registers and explain.
b) An 8-bit register contains the binary value 10011100. What is the register value after an Arithmetic Shift Right? Starting from the initial number 10011100, determine the register value after an arithmetic Shift Left, and state whether there is an overflow. [7+8]

2. Draw block diagram of a control memory and the associated hardware needed for selecting the next micro instruction address. [15]

3. Perform the arithmetic operation (+42)+(-13) and (-42)-(-13) in binary using signed 2's complement representation for negative numbers. [15]

4.a) Differentiate between Isolated I/O and memory-mapped I/O.
b) Explain programmed-I/O in detail. [8+7]

5.a) Write the major characteristics of RISC processors.
b) Draw a space-time diagram for a four-segment pipeline showing the time it takes to process six tasks and explain. [7+8]

6.a) Draw the flowchart for instruction cycle and explain.
b) Explain the following instructions: BUN, ISZ, BSA, LDA, STA. [7+8]

7. Explain various Data Manipulation instructions with examples. [15]

8. With an example, explain Booth Multiplication algorithm. [15]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, September - 2021
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Draw the block diagram of a digital computer and explain the purpose of each part.
b) Design a 4-bit combinational circuit decrementer using four full-adder circuits. [6+9]

2. What are the common fields found in instruction format? Explain various instruction formats based on types of CPU Organization? [15]

3. Perform the arithmetic operation (+41)+(-13) and (-41)-(-13) in binary using signed 2's complement representation for negative numbers. [15]

4.a) Draw the block diagram of a typical DMA controller and explain.
b) Explain Daisy-Chain priority interrupt in detail. [8+7]

5.a) Construct a diagram for a 4×4 omega Switching network. Show the switch setting required to connect input 3 to output 1.
b) Give a brief note on mutual exclusion with a semaphore. [9+6]

6.a) Differentiate between computer organization and computer architecture.
b) Explain the Stored Program organization in detail. [7+8]

7. Explain the microprogram sequencer for a control memory with a neat diagram. [15]

8. Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in the signed-2's complement representation. [15]

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