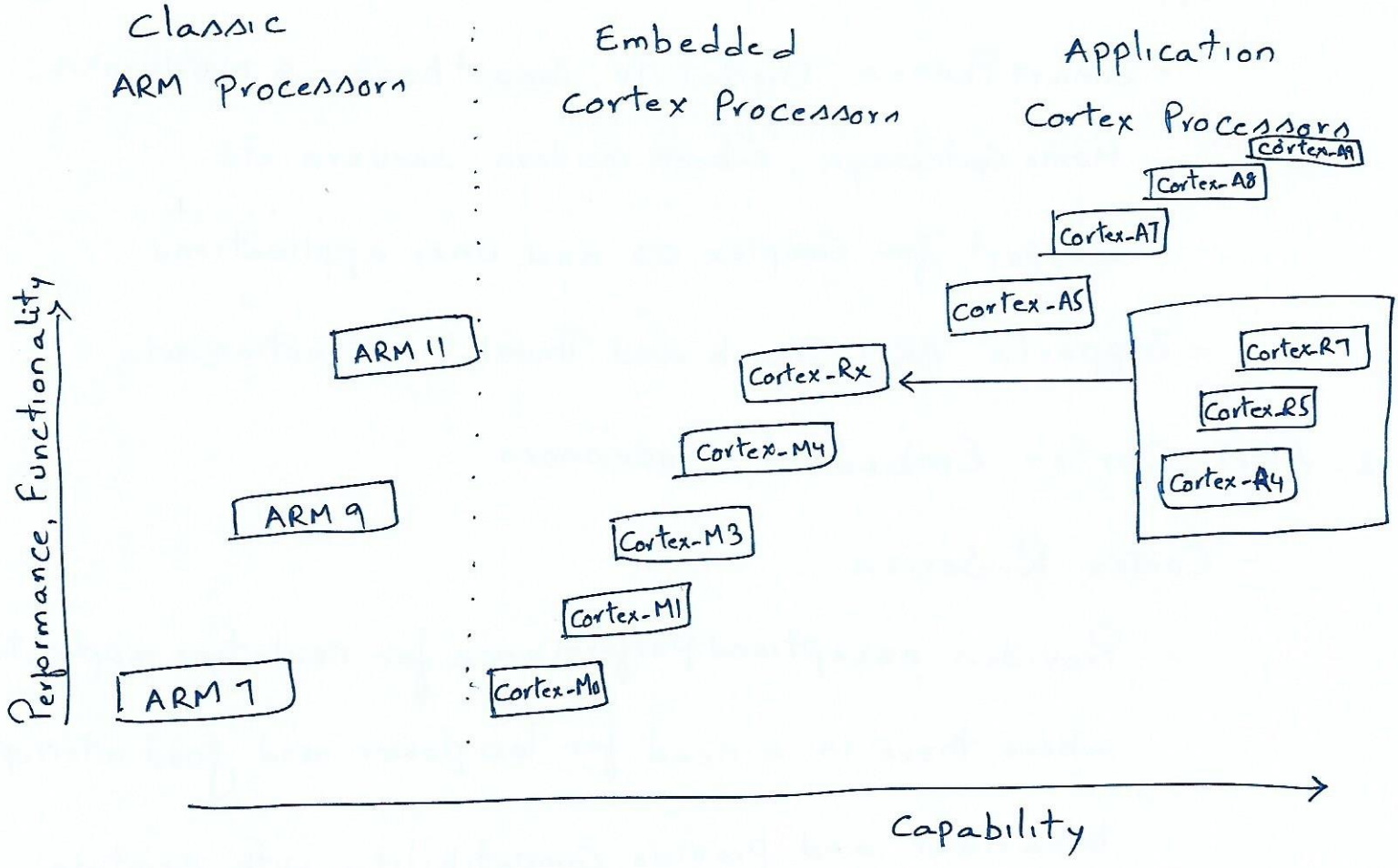
mood-book

Introduction to ARM Cortex Processors

- Cortex is an advanced microcontroller in ARM family, developed by ARM V7 architecture
- Cortex family is sub-divided into three sub-families
  - ARM CORTEX Ax-Series
  - ARM CORTEX Rx-Series
  - ARM CORTEX Mx-Series

x indicates a number that identifies in detail the Core

- These ARM families are divided into three macro families.



1. Cortex Application Processor

- Cortex_A-Series

  - These processors deliver exception Performance upto 2 GHZ+ typical frequency in advanced process nodes, enabling the next generation of mobile internet devices

  - These processors are available in Single-Core and multi-Core Varities, delivering upto 4 processing units with option NEON multimedia processing ~~tools~~ blocks and advanced Floating point execution units

  Applications

  - Smart Phones, Digital TV, Smartbooks & Netbooks, Home Gateways, e-book readers, Servers etc.

  - Support for Complex OS and user applications

  - Supports ARM, Thumb and Thumb 2 instruction sets

2. ARM Cortex Embedded Processors

- Cortex R-Series

  - Provides exceptional Performance for real-time applications where there is a need for low power and good interrupt behaviour and provide Compatibility with existing platforms.

Applications - Automotive braking systems,
Power train solutions
Mass Storage Controller (Disk Drives)
Networking & Printing, Digital Cameras etc

- Supports ARM, Thumb and Thumb-2 instruction sets
- Cortex - Rx delivers a road map from classic ARM processors including ARM11, enabling existing applications to be easily ported to a higher performance platform

Cortex M-Series

- Cost sensitive solutions for deterministic microcontroller applications where the need for fast, highly deterministic, interrupt management is coupled with the desire for extremely low gate count and lowest possible power consumption.

Applications - Microcontrollers, Mixed Signal Devices, Smart Sensors, Automotive body electronics and airbags

Cortex Mx is divided into four subgroups, that are M0, M1, M3 and M4. The power consumption of CORTEX Mx is in the range of 0.84 DMIPS/MHZ to 1.25 DMIPS/MHZ

Embedded processors are primarily focused on high deterministic real time behavior with power sensitivity and often execute an RTOS alongside user-developed application code and hence requires a memory protection unit (MPU) as opposed to MMU in application processors

Comparison of Cortex - A processors family

ARM Core	A5	A7	A8	A9
Year of Establishment	2009	2011	2005	2007
ARM Architecture	ARM V7	ARM V7	ARM V7	ARM V7
No. of Instruction Pipeline stages	8	8	13 (integer) 10 (NEON)	8
External interfaces used	AMBA AXI APB DFT	ACE APB DFT MBIST	AMBA AXI AMBA APB AMBA ATB DFT	AMBA AXI Debug V7-Complaint Interface DFT

ATB - Advanced Trace Bus

APB - Advanced Peripheral Bus

Comparison of Cortex-R family of Processors

ARM Core	R4	R5	R6	R7
Year of Establishment	2011	2011	2011	2016
ARM Architecture	ARMV7	ARMV7	ARMV7	ARMV7
Memory Architecture	Harvard	Harvard	Harvard	Harvard
No. of Instruction Pipeline stages	8	8	11	8
Max. Clock frequency	>1.4GHz	>1.4GHz	>1.5GHz	>1.5GHz

Comparison of ARM Cortex-M family of Processors

ARM Core	M0	M1	M3	M4	M7
Year of Establishment	2009	2007	2004	2010	2014
ARM Architecture	ARMV6-M	ARMV6-M	ARMV7-M	ARMV7E-M	ARMV7E-M
Memory Architecture	Von-Neuman	Von-Neuman	Harvard	Harvard	Harvard
No-of instruction Pipeline stages	3	3	3	3	6
Interrupts	1 to 3 (NMI)	1 to 32 (NMI)	1 to 240 (NMI)	1 to 240 (NMI)	1 to 240 (NMI)
Interrupt Latency	16 cycles	23 for NMI 26 for IRQ	12 cycles	12 Cycles	12 Cycles
Microcontroller chips based on	Toshiba TX00 NXP LPC 1100 Cypress 4M PSOC 4	Xilinx Spartan-3 Altera Cyclone-II IGLOO/e	NXP LPC 1300 Toshiba TX03 Actel Smart fusion	Toshiba X4 NXP V3 cypress PSOC6	Microchip SAME 70 NXP Kinetics Kv5x

Harvard vs Von-Neumann Architecture

Harvard	Von-Neumann
1. Seperate buses for instruction and data fetching	1. Single shared bus for instruction anddata fetching
2. Easy to pipelne, so high performance can be acheived	2. Low performance compared to Harvard
3. Comparatively High Cost	3. Cheaper

Harvard	Von-Neumann
4. No memory alignment problems	4. Allows self modifying Codes
5. Since data memory and Program memory are stored physically in different locations, no chances for accidental corruption of Program memory	5. Since data memory and program memory are stored physically in the same chip, chances for accidental corruption of Program memory.

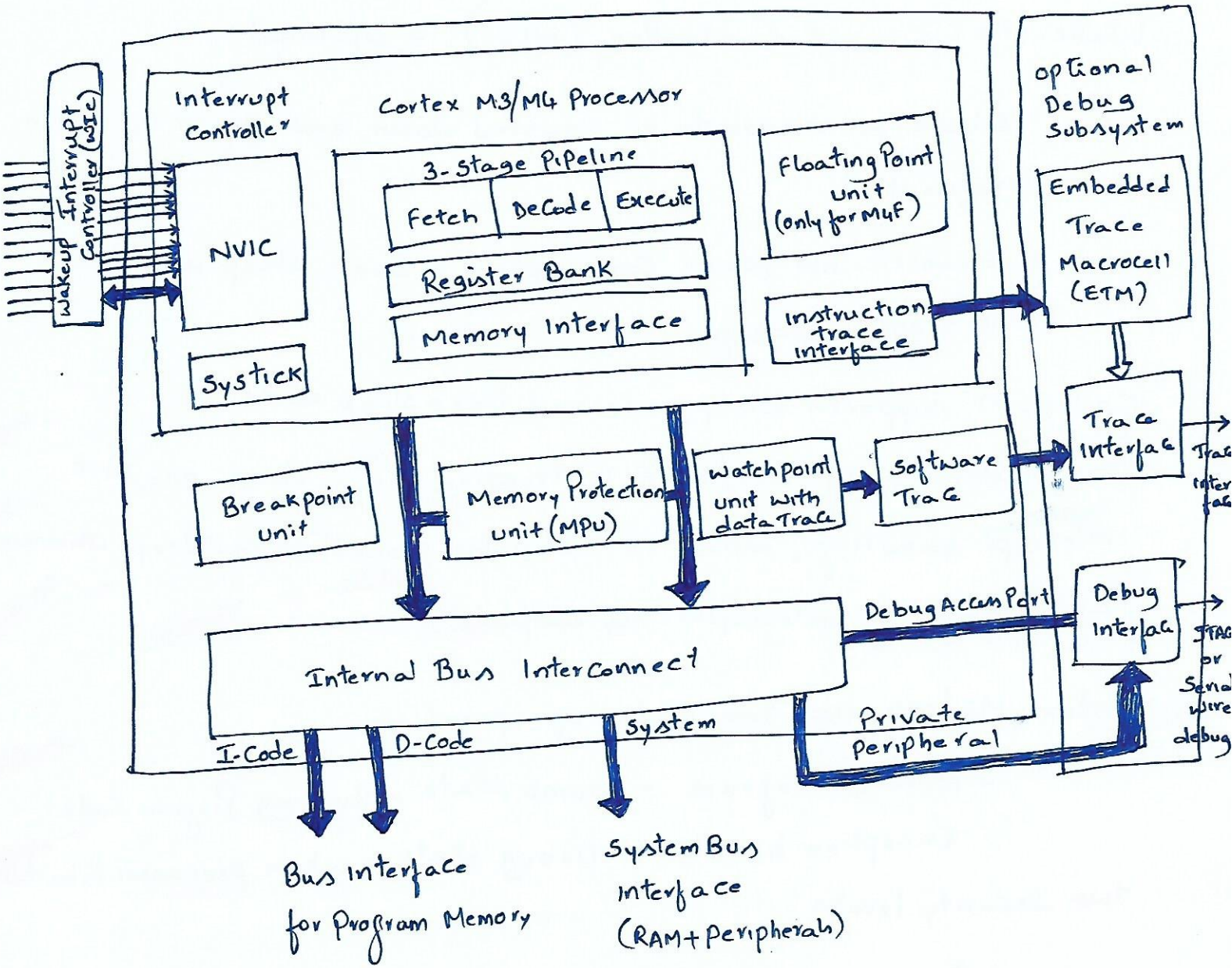
ARM Cortex-M Architecture

(Typically M3 & M4 are most succesful)

Features of M3 & M4

- 32 bit registers
- 32 bit internal data Path
- 32 bit Bus Interface unit
- Thumb ISA (instruction set architecture) - Thumb 2
- Three stage pipeline Design including branch forwarding & speculation
- Harvard architecture with Unified memory space
- 32 bit addressing, supporting 4 GB of memory space
- Onchip bus interfaces based on ARM AMBA (Advanced Micro Controller Bus Architecture)
- An interrupt Controlled called NVIC (Nested Vector interrupt Controller) supporting upto 240 interrupt requests and 8 to 256 interrupt priority levels.

- Supports for various features for OS implementation such as systemtic timer, shadowed stack pointer etc
- Sleep mode support and various low power features
- Support for an optional Memory Protection Unit (MPU) to Provide memory protection features like programmable memory or access permision Control.



Nested Vectored Interrupt Controller (NVIC)

- Faster interrupt response with less software effort
- 12 cycles, deterministic and low latency

- Interrupt Service Routines are standard C functions
- Interrupt table is simply a set of pointers to C routines
- An integrated NVIC handles
  - Saving Corruptible registers
  - Exception prioritization
  - Exception Nesting

Wake-Up Interrupt Controller (WIC) - optional

- Allows processor to be powered down and power up when requested
- Enables nW power consumption in deep sleep mode with instant wake up.

- Cortex-M supports sleep mode and Deep sleep mode.
- Enter sleep using WFI/WFE instruction or "sleep-on-Exit" interrupt handling, which enables the processor to sleep whenever all outstanding interrupts are Complete

Cortex-M3/M4 has two modes of operation

- Normal Program - Thumb state - Running Program Code
- Exception handler - Debug state - when processor is halted

two Security levels

- Basic security model - Can access all resources in the Processor
- Memory Access Protection - Few memory regions & few operation not available

- Register File is similar to traditional ARM but with reduced area.
- In this case there are two stack pointers, namely, Main and Process.

With Thumb-2 technology, Cortex-M has a no. of advantages

- No state switching overhead, saving both execution time and instruction space
- No need to specify ARM state or Thumb state
- Easy to get best ~~Sacr~~Code density, efficiency and performance at the same time

Cortex Processors do not come with memories included. The vendor adds them as

Program Memory - Typically Flash

Data Memory - Typically SRAM

Peripherals

Cortex-M implements Bit Banding, a method of performing atomic bitwise modifications to memory i.e., preventing data loss while interrupted during a read-modify-write cycle

Memory Protection Unit (optional)

- Has eight memory regions
- Sub region Disable, enabling efficient use of memory regions
- Ability to enable a background region that implements the default memory map attributes

Floating Point Unit (FPU) - Optional

- 32 dedicated 32-bit instructions for single-precision data-processing instructions (addressable as 16 double word registers)
- Combined Multiply and Accumulate instructions for increased Precision

- Hardware Support for Conversion, addition, subtraction, multiplication with optional accumulate, division and squareroot

- Decoupled three stage pipeline

Low Cost Debug Subsystem (optional)

- Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the Core is halted and access to debug control registers even when SYSRESETn is asserted.

Embedded Trace Macrocell (ETM) - For instruction trace

Trace Interface Unit (TIU) - For bridging to a trace port analyzer including single wire output mode

Instrumentation Trace Macrocell (ITM) - Support for Printf style debugging

Data Watch Point and Trace (DWT) - For implementing watchpoints, data tracing and system profiling

Flash Patch and Break Point (FPB) - Implementing breakpoints & Patches

Serial Wire Debug / JTAG Debug port - Debug Access

Bus Interfaces

Processor contains four AHB (Advanced High Performance Bus) Lite Bus interfaces

Private Peripheral Bus (PPB)

- Data and debug access to external PPB space, 0xE0040000 to 0xE00FFFFF are performed over Advanced Peripheral Bus (APB)
- Trace Port interface unit and Vendor specific peripherals are on the bus.
- Core data accesses have higher priority than debug accesses
- Only address bits necessary to decode the external PPB are supported on this interface.

ETM Interface

- Simple Connection of ETM to the processor
- Provides a channel for instruction trace to ETM

AHB Trace Macrocell Interface

- Enables connection of AHB trace macrocell to processor
- Provides channel for Data trace to HTM

Debug Port AHB-AP interface

- Processor Contains AHB-AP interface for debug accesses through an external debug Port
- Serial wire JTAG debug port is a standard Core sight debug Port that Combines JTAG-DP and SW-DP (2 pin interface to AHB-AP)

I Code Memory Interface

- Instruction fetches from code memory space, 0x00000000 to 0x1FFFFFFF are performed over this 32-bit bus
- Debugger cannot access this interface
- All fetches are word-wide
- No. of inst. fetched per word depends on the Code running and alignment of Code in memory

D Code Memory Interface

- Data and debug access ~~from~~ to Code memory space, 0x00000000 to 0x1FFFFFFF are performed over this bus.
- Core data has higher priority over debug accesses
- Control logic in this interface converts unaligned data and debug accesses into two or three aligned accesses depending on the size and alignment of unaligned access
- DCode has higher priority than ICode

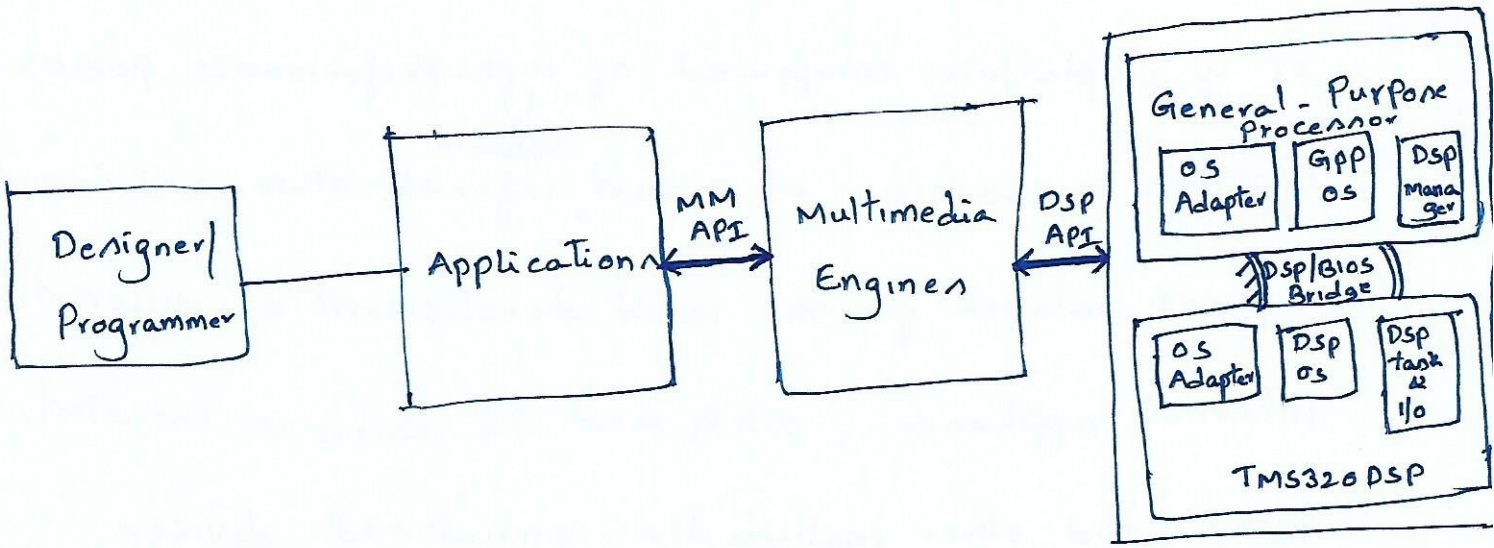
System Interface

- Instruction fetches, and data and debug accesses to address ranges 0x20000000 to 0xDFFFFFFF and 0xE0100000 to 0xFFFFFFFF are performed over this bus
- The order in decreasing priority for accessing this bus is
  - Data Accesses
  - Instruction and Vector fetches
  - Debug

OMAP Processor - Open Mobile Application Processor

- It is a platform comprised of high-Performance, power efficient processors, a robust Software infrastructure and Comprehensive support network for the rapid development of differentiated internet appliances, 2.5G and 3G wireless handsets and PDAs and other multimedia-enhanced devices
- It is a Combination of DSP Core and high performance RISC processor
- The DSP processor is suitable for signal processing appln's such as speech recognition, MPEG4 Video & Audio playback.
- RISC processor is suitable for execution of Control instructions required for OS, man-machine interfaces and OS applications
- Major advantage of using two processors is to reduce the Consumption of power to a large extent i.e., greater battery life and also DSP is allowed to gain support from RISC processor.

OMAP Architecture



1. Designer programs OMAP's dual processor platform as though addressing a single processor (integrates ARM RISC & Texas Inst. TMS320C DSP)
2. OMAP uses standard programming interfaces (API's) for user friendly application development
3. Multimedia engines make use of proxies for related DSP tasks in the GPP domain
4. DSP/BIOS bridge Coordinates data, I/O streams and DSP task Control between the proxies and the actual DSP Software to maximize performance without sacrificing battery Power.

Other Features

- OMAP application environment is fully programmable that allows wireless device OEM's (original Equipment Manufacturer) independent developers and Carriers to provide downloadable software. upgrades as standards change or bugs are found.

- No need to develop new ASIC hardware to implement changes
- OMAP has an open architecture with standardized interface, and encourages third-party developers to create new applications
- Integrating available third party and OS native tools with TI's user friendly Code Composer Studio (CCS) integrated development environment (IDE) makes complete software development available for OMAP H/W & S/W.

DSP Advantage

- DSP's provide superior power/performance in Video & Audio applications as they are signal processing tasks and DSP's are optimized for such type of applications only and require less power per cycle than RISC
- Programmable DSP's allow developers to implement any available standard without creating unacceptable battery drain
- DSP requires fewer instructions to implement a math-intensive repetitive algorithm, and it carries out more instructions Per clock cycle resulting in faster implementation with less Power Consumption.

Coupling DSP with RISC

- OMAP architecture gives OEM's access to capabilities of DSP's while also providing command and control functions for which Risc processors are best suited.

Advantage : Improves quality of basic wireless telephony functions and permits true multimedia multitasking on wireless appliances.

DSP/BIOS Bridge

- Provides application software developer, a seamless easy to use interface to the DSP.
- It allows developer on the RISC to access and control the DSP runtime environment using a standardized API
- No need for the developer to program for two processors independently or to work in more difficult language environment sometimes associated with DSP's

Open Architecture

- once an application is developed for OMAP using standardized API, it will be compatible with future end equipments based on OMAP architecture, maximizing reuse.
- TI supports Java in OMAP architecture and makes DSP/BIOS bridge API accessible to developers of java media players