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Code No: 153AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**B. Tech II Year I Semester Examinations, April/May - 2023****ANALOG AND DIGITAL ELECTRONICS****(Common to CSE, IT, ECM, ITE, CE(SE), CSE(CS), CSE(N))****Time: 3 Hours****Max. Marks: 75****Note:** i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A**(25 Marks)**

- 1.a) Give the applications of PN junction diode. [2]
- b) Discuss about diode switching times. [3]
- c) Discuss about gain bandwidth product in amplifier using BJT. [2]
- d) What is thermal runaway? [3]
- e) Define de morgan laws. [2]
- f) Define the pinch-off voltage. Why the name field effect is used for the device FET? [3]
- g) Differentiate between encoder and decoder. [2]
- h) How Decimal Adder different from Binary adder? [3]
- i) What is excitation table? Write the excitation tables for the SR flip flop. [2]
- j) What is state assignment? Explain with a suitable example. [3]

PART – B**(50 Marks)**

- 2.a) Define and derive the equation for diffusion capacitance.
 - b) Explain positive and negative diode clipper circuits. [4+6]
- OR**
- 3.a) Briefly discuss about PN junction diode and light emitting diode.
 - b) Discuss about half wave rectifier with and without capacitive filter. [5+5]
- 4.a) Explain the input and output characteristics of a transistor in CE configuration.
 - b) Draw a Self-bias circuit and explain its operation. Derive the equation for Stability factor. [5+5]
- OR**
- 5.a) Explain various methods used for coupling of multistage amplifiers with their frequency response.
 - b) Draw and explain equivalent circuit of transistor at low frequencies. [6+4]
- 6.a) Draw the circuit diagram of common drain amplifier and derive expression for voltage Gain using FET .
 - b) Simplify the following function and realize using universal gates
$$F(A,B,C) = A'BC' + ABC + B'C' + A'B'$$
 [5+5]

OR

- 7.a) Explain the construction and principle of operation of Enhancement mode N-channel MOSFET.
b) Explain the operation of TTL with neat diagram. [5+5]

- 8.a) Minimise the following Boolean function using K-map and design a logic circuit using NAND gates.

$$F = \sum m(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$$

- b) Construct a 3*8 decoder using logic gates and its truth table. [5+5]

OR

- 9.a) Express the function $(xy+z)(y+xz)$ in canonical SOP and POS forms.

- b) Implement the following Boolean function with a multiplexer.

$$F(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 14, 15) \quad [5+5]$$

- 10.a) Draw and explain the logic diagram of 4-bit ring counter with the help of timing diagrams.

- b) Realize D-FF and T-FF using JK-FF. [5+5]

OR

- 11.a) Explain about the universal shift registers.

- b) Discuss in detail about various types of ROM. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, August/September - 2022

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT, ECM, ITE, CSE(SE), CSE(CS), CSE(N))

Time: 3 Hours

Max.Marks:75

Answer any five questions
All questions carry equal marks

- 1.a) Discuss the different types of junction breakdowns that can occur in a reverse biased diode.
- b) Explain operation of diode in forward bias and reverse bias condition. Draw V-I characteristics of diode. [8+7]
- 2.a) Explain about the full-wave center-tap rectifier with L section filters and also draw suitable diagram and waveforms.
- b) Write a short note on diffusion capacitance and diode switching times. [8+7]
- 3.a) With neat diagrams and necessary equations, explain the effect of coupling capacitor and bypass capacitor on the performance of an amplifier at low-frequencies?
- b) Explain how self-biasing can be done in a BJT with relevant sketches and waveforms? [8+7]
- 4.a) Write equations of voltage gain, current gain, Input impedance and Output impedance of CE amplifier.
- b) Explain how transistor acts as an amplifier? [10+5]
- 5.a) Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers.
- b) With the help of a neat schematic, explain the functioning of a common drain amplifier. [8+7]
- 6.a) Define the De Morgan Laws with suitable example.
- b) Implement the basic logic gates by using modified DTL gates, HTL and TTL gates. [6+9]
- 7.a) Explain the function of a Encoder with necessary diagrams and discuss its applications.
- b) Design the 4-bit binary Adder-Subtractor with suitable diagram. [6+9]
- 8.a) Give the design of 3 bit Ring counter and explain its operation with waveforms. Also give the applications of ring counter.
- b) Obtain the characteristic equations of D and T flip flops. [9+6]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**B.Tech II Year I Semester Examinations, March - 2021****ANALOG AND DIGITAL ELECTRONICS**

(Common to CSE, IT, ITE)

Time: 3 hours**Max. Marks: 75****Answer any five questions
All questions carry equal marks**

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- 1.a) Derive the expression for ripple for the circuit FWR with inductor filter.
b) Explain the working of semiconductor photo diode. [8+7]
- 2.a) Explain V-I characteristics of a tunnel diode and write its applications.
b) Define clipping and clamping circuits. Differentiate clipping and clamping circuits. [7+8]
- 3.a) Draw the circuit diagram of an NPN junction transistor in CE configuration and describe its characteristics.
b) For the transistor amplifier circuit, when signal changes by 0.012 V, the base current changes by 9 μ A and collector current by 1.3 mA. If the collector load $R_C = 6 \text{ K}\Omega$, $R_L = 12 \text{ K}\Omega$. Determine input resistance, current gain and voltage gain. [9+6]
- 4.a) What is the necessity of biasing circuits? Derive the expression for stability factor of self-bias circuit.
b) Derive the expressions for Z_i , Z_o and A_v for common drain J-FET amplifier. [8+7]
- 5.a) Draw a totem-pole output buffer with a TTL gate. Explain its operation.
b) Draw the circuit of an improved version of D.T.L. 3-input NAND gate, and explain its operations with the help of Truth Table. If h_{FE} of each transistor is 40, find FAN-OUT of the circuit. [8+7]
- 6.a) Simplify the following function using K-map.
 $F(A,B,C,D) = \Sigma(1,3,4,5,6,11,13,14,15)$
b) Draw the logic circuit of a 3 to 8 decoder and explain its working. [7+8]
- 7.a) Design a 4-bit comparator circuit using logic gates.
b) Design a modulo 10 counter using JK flipflops and explain its timing diagram. [7+8]
- 8.a) Using D-Flip flops and waveforms, explain the working of a 4-bit SISO shift register.
b) Difference between static and dynamic RAM. Draw the circuits of one cell of each and explain its working. [7+8]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, March - 2022

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT, ECM, ITE, CSE(SE), CSE(CS), CSE(N))

Time: 3 Hours

Max. Marks: 75

Answer any five questions
Each Carries Equal Marks

- 1.a) Explain the operation of PN junction under forward bias condition with its characteristics.
- b) Describe the operation of Half Wave Rectifier with and without filters. [7+8]
- 2.a) Explain about RC coupled amplifier and sketch the frequency response plot of an RC coupled amplifier
- b) A transistor operating in CB configuration has $I_C = 2.98\text{mA}$, $I_E = 3.00\text{ mA}$ and $I_{CO} = 0.01\text{ mA}$. What current will flow in the collector circuit of this transistor when connected in CE configuration with a base current of $30\mu\text{A}$. [10+5]
- 3.a) What is thermal runaway? What is the condition for thermal stability in CE configuration?
- b) Derive the expression for stability factor S in self-bias circuit. [8+7]
- 4.a) Explain the operation of JFET and draw the drain and transfer characteristics.
- b) Explain about 2 input TTL NAND Gate. [10+5]
- 5.a) Convert the decimal number $(128.25)_{10}$ into binary, octal, hexadecimal number system.
- b) Build basic gates AND, NOT, OR using NAND and NOR gates. [6+9]
- 6.a) Simplify the following Boolean expression into one literal. $W'X(Z'+YZ) + X(W+Y'Z)$.
- b) What is multiplexer? Draw circuit diagram of 8:1 multiplexer. Explain its working in brief. [6+9]
- 7.a) Design a full subtractor circuit by using K-map method and draw the logic diagram.
- b) Explain 4-bit ring counter with circuit diagram and waveforms. [8+7]
- 8.a) Draw the logic diagram of clocked RS flip-flop using NAND gates and explain its working.
- b) With a neat diagram, explain 3-bit parallel in serial out shift register. [7+8]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, October - 2020

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT)

Time: 2 hours

Max. Marks: 75

Answer any five questions

All questions carry equal marks

- 1.a) Define Diffusion capacitance? Also derive the expression for C_D ?
b) Draw and explain the V-I characteristics of a tunnel diode? [8+7]
- 2.a) What is LED? Explain the construction of LED in brief?
b) Explain the working of a full wave rectifier with necessary waveforms? [7+8]
- 3.a) Explain the input and output characteristics of common base configuration.
b) Explain thermal run away and thermal stability. [8+7]
4. Analyse CE-CE amplifier in terms of gains and Impedances. [15]
- 5.a) Draw and explain the CS amplifier with current source load.
b) Explain the small signal MOSFET circuit model. [8+7]
- 6.a) Explain ECL gate and write the advantages and disadvantages.
b) Draw CMOS NOT gate and then explain the same. [8+7]
7. Simplify the following Boolean function using Quine – McClusky method.
 $F(A, B, C, D) = \sum m (0, 2, 3, 6, 7, 8, 10, 12, 13)$ [15]
- 8.a) What is state assignment? Explain with a suitable example?
b) Realize D and T flip flops using Jk flip flops. [8+7]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, September - 2021

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT, ITE)

Time: 3 hours

Max. Marks: 75

Answer any five questions

All questions carry equal marks

- 1.a) Explain the characteristics and applications of a photodiode.
b) How does the reverse saturation current of a diode varies with temperature? Explain. [7+8]
- 2.a) Draw a circuit diagram of series inductor filter with half wave rectifier. Explain with input and output waveforms.
b) Explain negative peak clipper with and without reference voltage. [8+7]
- 3.a) Explain self bias. Derive the expression for S? Why it is widely used.
b) Prove that the transistor acts as an amplifier with suitable circuit diagram. [7+8]
4. Derive the expression for A_{vs} , A_{is} , R_i , R_o of transistor amplifier using CB configuration. [15]
- 5.a) Explain the operation and characteristics of N- channel JFET.
b) Discuss any two applications of FET. [8+7]
- 6.a) Explain about Transistor–Transistor logic. Also mention the types of output configuration.
b) Prove that AND-OR network is equivalent to NAND-NAND network. [8+7]
- 7.a) Give the simplest logic circuit for following logic equation where d represents don't care conditions.
$$F(A,B,C,D) = \sum m(7) + d(10, 11, 12, 13, 14, 15).$$

b) Design a 32:1 multiplexer using 16:1 Mux and 2:1 multiplexer? [9+6]
- 8.a) Explain 4 bit parallel in serial out shift register.
b) Explain about RAM with neat sketches. [8+7]

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